

Analog to Digital Conversion

ADC TYPES

Analog-to-Digital Converters (ADCs) transform an analog voltage to a binary number (a series of 1's and 0's), and then eventually to a digital number (base 10) for reading on a meter, monitor, or chart. The number of binary digits (bits) that represents the digital number determines the ADC resolution. However, the digital number is only an approximation of the true value of the analog voltage at a particular instant because the voltage can only be represented (digitally) in discrete steps. How closely the digital number approximates the analog value also depends on the ADC resolution.

A mathematical relationship conveniently shows how the number of bits an ADC handles determines its specific theoretical resolution: An n-bit ADC has a resolution of one part in 2^n . For example, a 12-bit ADC has a resolution of one part in 4,096, where $2^{12} = 4,096$. Thus, a 12-bit ADC with a maximum input of 10 VDC can resolve the measurement into $10 \text{ VDC} / 4096 = 0.00244 \text{ VDC} = 2.44 \text{ mV}$. Similarly, for the same 0 to 10 VDC range, a 16-bit ADC resolution is $10 / 2^{16} = 10 / 65,536 = 0.153 \text{ mV}$. The resolution is usually specified with respect to the full-range reading of the ADC, not with respect to the measured value at any particular instant.

Successive-Approximation ADCs

A successive-approximation converter, Figure 2.01, is composed of a digital-to-analog converter (DAC), a single comparator, and some control logic and registers. When the analog voltage to be measured is present at the input to the comparator, the system control logic initially sets all bits to zero. Then the DAC's most significant bit (MSB) is set to 1, which forces the DAC output to 1/2 of full scale (in the case of a 10-V full-scale system, the DAC outputs 5.0 V). The comparator then compares the analog output of the DAC to the input signal, and if the DAC output is lower than the input signal, (the signal is greater than 1/2 full scale), the MSB remains set at 1. If the DAC output is higher than the input signal, the MSB resets to zero. Next, the second MSB with a weight of 1/4 of full scale turns on (sets to 1) and forces the output of the DAC to either 3/4 full scale (if the MSB remained

at 1) or 1/4 full scale (if the MSB reset to zero). The comparator once more compares the DAC output to the input signal and the second bit either remains on (sets to 1) if the DAC output is lower than the input signal, or resets to zero if the DAC output is higher than the input signal. The third MSB is then compared the same way and the process continues in order of descending bit weight until the LSB is compared. At the end of the process, the output register contains the digital code representing the analog input signal.

Successive approximation ADCs are relatively slow because the comparisons run serially, and the ADC must pause at each step to set the DAC and wait for its output to settle. However, conversion rates easily can reach over 1 MHz. Also, 12 and 16-bit successive-approximation ADCs are relatively inexpensive, which accounts for their wide use in many PC-based data acquisition systems.

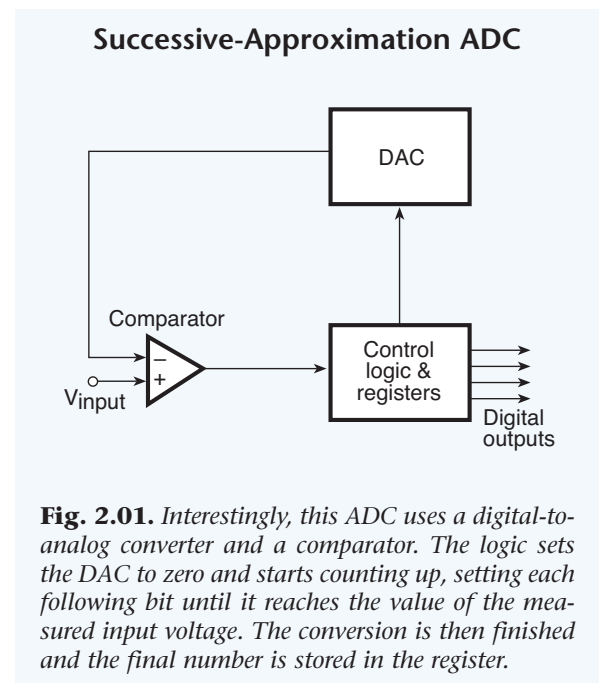


Fig. 2.01. Interestingly, this ADC uses a digital-to-analog converter and a comparator. The logic sets the DAC to zero and starts counting up, setting each following bit until it reaches the value of the measured input voltage. The conversion is then finished and the final number is stored in the register.

Voltage-to-Frequency ADC

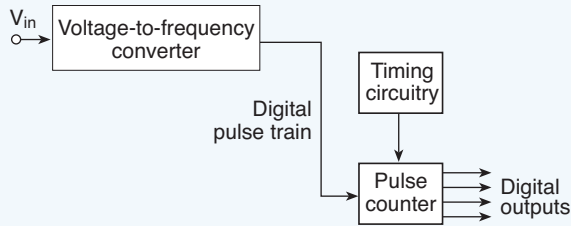


Fig. 2.02. Voltage-to-frequency converters reject noise well and frequently are used for measuring slow signals or those in noisy environments.

Voltage-to-Frequency ADCs

Voltage-to-frequency ADCs convert the analog input voltage to a pulse train with the frequency proportional to the amplitude of the input. (See Figure 2.02.) The pulses are counted over a fixed period to determine the frequency, and the pulse counter output, in turn, represents the digital voltage.

Voltage-to-frequency converters inherently have a high noise rejection characteristic, because the input signal is effectively integrated over the counting interval. Voltage-to-frequency conversion is commonly used to convert slow and noisy signals. Voltage-to-frequency ADCs are also widely used for remote sensing in noisy environments. The input voltage is converted to a frequency at the remote location and the digital pulse train is transmitted over a pair of wires to the counter. This eliminates noise that can be introduced in the transmission lines of an analog signal over a relatively long distance.

Integrating ADCs: Dual Slope

A number of ADCs use integrating techniques, which measure the time needed to charge or discharge a capacitor in order to determine the input voltage. A widely used technique, called dual-slope integration, is illustrated in Figure 2.03. It charges a capacitor over a fixed period with a current proportional to the input voltage. Then, the time required to discharge the same capacitor under a constant current determines the value of the input voltage. The technique is relatively accurate and stable because it depends on the ratio of rise time to fall time, not on the absolute value of the capacitor or other components whose values change over temperature and time.

Integrating the ADC input over an interval reduces the effect of noise pickup at the ac line frequency when the integration time is matched to a multiple of the ac period. For this reason, it is often used in precision digital multimeters and panel meters. Although 20-bit accuracy is common, it has a relatively slow conversion rate, such as 60 Hz maximum, and slower for ADCs that integrate over multiples of the line frequency.

Sigma-Delta ADCs

A sigma-delta ADC is another type of integrating ADC. It contains an integrator, a DAC, a comparator, and a summing junction. (See Figure 2.04.) Like the dual-slope ADC, it's often used in digital multimeters, panel meters, and data acquisition boards. Sigma-delta converters are relatively inexpensive primarily because

Dual-Slope ADC Integration and Discharge Times

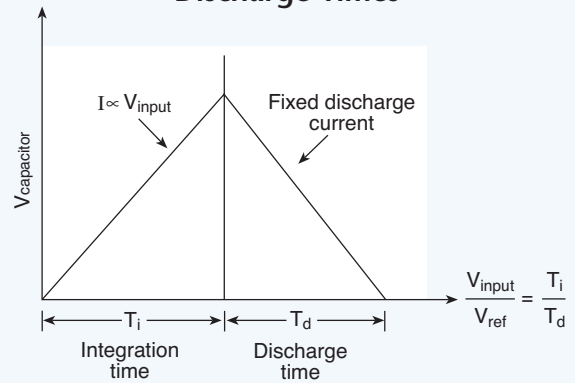


Fig. 2.03. Dual-slope integrating ADCs provide high-resolution measurements with excellent noise rejection. They integrate upward from an unknown source voltage and then integrate downward with a known source voltage. They are more accurate than single slope ADCs because component errors are washed out during the de-integration period.

they have a single-bit DAC, but they can obtain high-resolution measurements using oversampling techniques. Although the ADC works best with low-bandwidth signals (a few kHz), it typically has better noise rejection than many others, and users can set the integration time (albeit below 100 samples/sec).

Sigma-delta ADCs also require few external components. They can accept low-level signals without much input-signal conditioning circuitry for many applications, and they don't require trimming or calibration components because of the DAC's architecture. The ADCs also contain a digital filter, which lets them work at a high oversampling rate without a separate anti-aliasing filter at the input. Sigma-delta ADCs come in 16 to 24-bit resolution, and they are economical for most data acquisition and instrument applications.

Sigma-Delta ADC

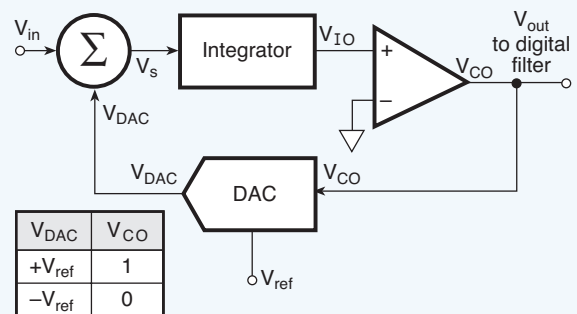


Fig. 2.04. Integrating converters such as the sigma-delta ADC have both high resolution and exceptional noise rejection. They work particularly well for low-bandwidth measurements and reject high-frequency noise as well as 50/60 Hz interference.

Sigma-Delta ADC With Digital Filter and Decimator Stage

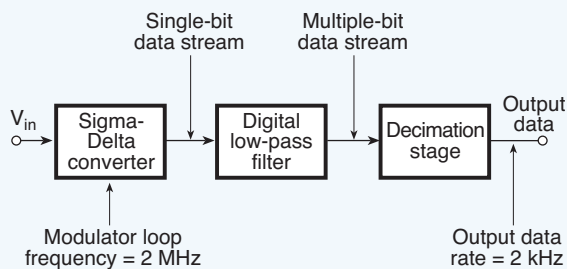


Fig. 2.05. Sigma-delta ADCs are well suited to high-resolution acquisition because they use oversampling and often combine an analog modulator, a digital filter, and a decimator stage. The low-pass digital filter converts the analog modulator output to a digital signal for processing by the decimator.

The principle of operation can be understood from the diagram. The input voltage V_{in} sums algebraically with the output voltage of the DAC, and the integrator adds the summing point output V_S to a value it stored previously. When the integrator output is equal to or greater than zero, the comparator output switches to logic one, and when the integrator output is less than zero, the comparator switches to logic zero. The DAC modulates the feedback loop, which continually adjusts the output of the comparator to equal the analog input and maintain the integrator output at zero. The DAC keeps the integrator's output near the reference voltage level. Through a series of iterations, the output signal becomes a one-bit data stream (at a high sample rate) that feeds a digital filter. The digital filter averages the series of logic ones and zeros, determines the bandwidth and settling time, and outputs multiple-bit data. The digital low-pass filter then feeds the decimation filter, which in turn, decreases the sample rate of the multi-bit data stream by a factor of two for each stage within the filter. For example, a seven-stage filter can provide a sample-rate reduction of 128.

Improved Accuracy

The digital filter shown in Figure 2.05 inherently improves the ADC's accuracy for ac signals in two ways. First, when the input signal varies (sine wave input) and the system samples the signal at several times the Nyquist value (refer to page 17), the integrator becomes a low-pass filter for the input signal, and a high-pass filter for the quantization noise. The digital filter's averaging function then lowers the noise floor even further, and combined with the decimation filter, the data stream frequency at the output is reduced. For example, the modulator loop frequency could be in the MHz region, but the output data would be in the kHz region. Second, the digital filter can be notched at 60 Hz to eliminate power line frequency interference.

The output data rate from the decimation filter is lower than the initial sample rate but still meets the Nyquist requirement by saving certain samples and eliminating others. As long as the output data rate is at least two times the bandwidth of the signal, the decimation factor or ratio M can be any integer value. For example, if the input is sampled at f_s , the output data rate can be f_s/M without

Table of ADC Attributes		
ADC Type	Typical Resolution	Typical Conversion Rate*/Frequency
Sigma-Delta	16–24 bit	1 sps–128 ksp/s
Successive Approximation	8–16 bit	10 ksp/s–2 Msp/s
Voltage-to-Frequency	8–12 bit	1 Hz–4 MHz**
Integrating	12–24 bit	1 sps–1 ksp/s**

* sps = samples per second
** With line cycle rejection

Fig. 2.06. Table of ADC attributes

losing information. This technique provides more stable readings. (Refer to the table in Figure 2.06 for ADC comparisons.)

ACCURACY AND RESOLUTION

Accuracy is one of the most critical factors to consider when specifying an ADC for test and measurement applications. Unfortunately, it's often confused with resolution, and although related, they are distinctly different. Both topics are discussed in this section in some detail, as well as their relationship to calibration, linearity, missing codes, and noise.

Accuracy vs. Resolution

Every ADC measurement contains a variety of unavoidable, independent errors that influence its accuracy. When σ_i represents each independent error, the total error can be shown as:

This equation includes a variety of errors such as sensor anomalies,

$$\sigma_{\text{total}} = \sqrt{\sum_i \sigma_i^2}$$

noise, amplifier gain and offset, ADC quantization (resolution error), and other factors.

Quantization Error

In a theoretically perfect ADC, any particular analog voltage measured should be represented by a unique digital code, accurate to an infinite number of digits. (See Figure 2.07A.) But in a real ADC, small but finite gaps exist between one digital number and a consecutive digital number, and the amount depends on the smallest quantum value that the ADC can resolve. In the case of the 12-bit converter covering a 10 VDC range, for example, that quantum value is 2.44 mV, the LSB. In other words, the input analog voltage range is partitioned into a discrete number of values that the converter can measure, which is also the ADC's resolution. The quantization error in this case is specified to be no more than half of the least significant bit (LSB). For the 12-bit ADC, the error is ± 1.22 mV (0.0122%). Such ADC errors are typically specified in three ways: the error in LSBs, the voltage error for a specified range, and the % of reading error. Most ADCs are not as accurate as their specified resolution, however, because other errors contribute to the overall error such as gain, linearity, missing codes, and offset. (See Figures 2.07B, C, D, and E, respectively). Nonetheless, the accuracy of a good ADC should approach its specified resolution.

Common ADC Errors

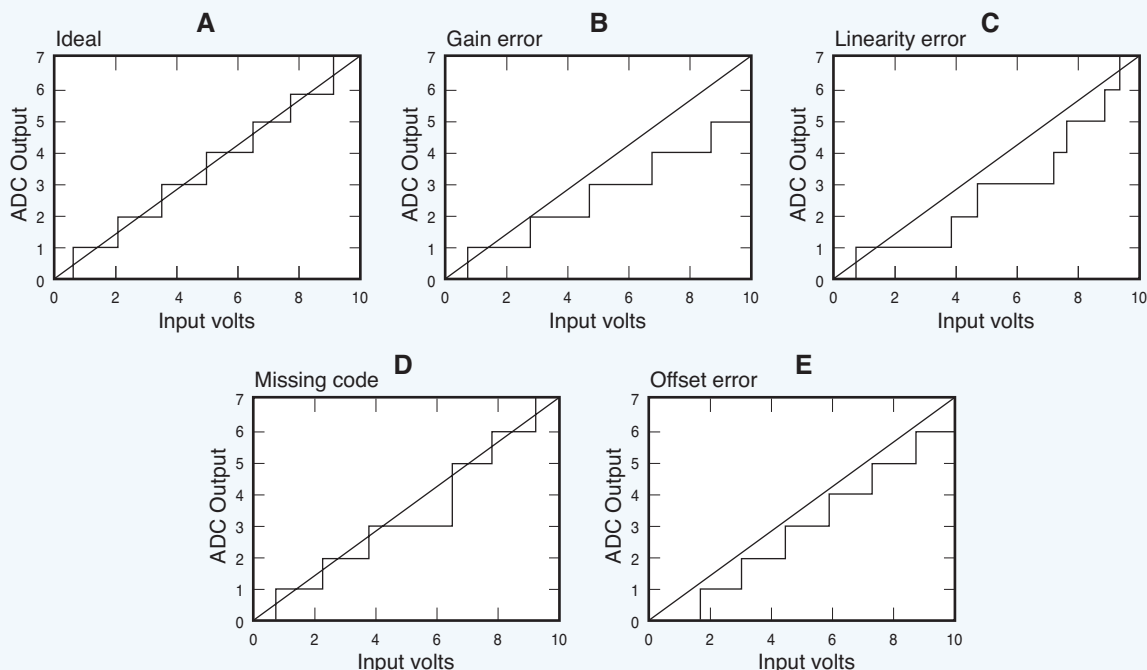


Fig. 2.07. The straight line in each graph represents the analog input voltage and the perfect output voltage reading from an ADC with infinite resolution. The step function in Graph A shows the ideal response for a 3-bit ADC. Graphs B, C, D, and E show the effect on ADC output from the various identified errors.

When an ADC manufacturer provides calibration procedures, offset and gain errors usually can be reduced to negligible levels, however, linearity and missing-code errors are more difficult or impossible to reduce.

ADC Accuracy vs. System Accuracy

Calibration

ADCs may be calibrated with hardware, software, or a combination of the two. Calibration in this case means adjusting the gain and offset of an ADC channel to obtain the specified input-to-output transfer function. In a hardware configuration, for example, the instrumentation amplifier driving the ADC has its offset and gain adjusted with trim pots, and changing the ADC's reference voltage changes its gain. In hardware/software calibrations, the software instructs DACs to null offsets and set full-scale voltages. Lastly, in a software calibration, correction factors are stored in nonvolatile memory in the data acquisition system or in the computer and are used to calculate the correct digital value based on the readings from the ADC.

ADCs are factory calibrated before being shipped, but time and operating temperature can change the settings. ADCs need to be recalibrated usually after six months to a year, and possibly more often for ADCs with resolutions of 16 bits or more. Calibration procedures vary, but all usually require a stable reference source and an indicating meter of (at least three times) greater accuracy than the device being calibrated. Offset is typically set to zero with zero input, and the gain is set to full scale with the precise, full-scale voltage applied to the input.

In many measurements, the input voltage represents only the physical quantity under test. Consequently, system accuracy might be improved if the complete measurement system is calibrated rather than its individual parts. For example, consider a load cell with output specified under a given load and excitation voltage. Calibrating individual parts means that the ADC, load cell, and excitation source accuracy tolerances are all added together. With this approach, the error sources of each part are added together and generate a total error that is greater than the error that can be achieved simply by calibrating the system with a known precision load and obtaining a direct relationship between the input load and ADC output.

Linearity

When the input voltage and the ADC output readings deviate from the diagonal line (representing infinite resolution) more than the ideal step function shown in Figure 2.07A, the ADC error is nearly impossible to eliminate by calibration. The diagonal line represents an ideal, infinite-resolution relationship between input and output. This type of ADC error is called a nonlinearity error. Nonlinearities in a calibrated ADC produce the largest errors near the middle of the input range. As a rule of thumb, nonlinearity in a good ADC should be one LSB or less.

Missing Codes

A quality ADC should generate an accurate output for any input voltage within its resolution, that is, it should not skip any successive digital codes. But some ADCs cannot produce an accurate digital output for a specific analog input. Figure 2.07D,

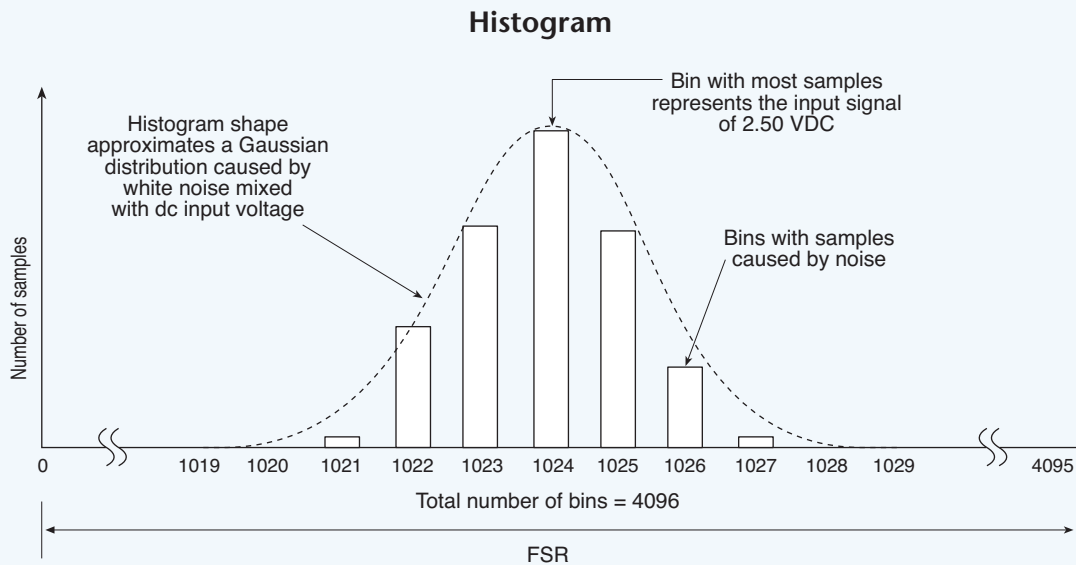


Fig. 2.08. The histogram illustrates how 12-bit ADC samples in a set were distributed among the various codes for a 2.5V measurement in a FSR (full-scale range) of 10V. Most codes intended for the 1024 bin representing 2.5V actually ended up there, but others fell under a Gaussian distribution due to white noise content.

for example, shows that a particular 3-bit ADC does not provide an output representing the number four for any input voltage. This type of error affects both the accuracy and the resolution of the ADC.

Noise

The cost of an ADC is usually proportional to its accuracy, number of bits, and stability. But even the most expensive ADC can compromise accuracy when excessive electrical noise interferes with the measured signal, whether that signal is in millivolts or much larger.

For example, many ADCs that reside on cards and plug into a PC expansion bus can encounter excessive electrical noise that seriously affects their accuracy, repeatability, and stability. But an ADC does not have to be connected directly to the bus within the computer. An ADC mounted in an external enclosure often solves the problem. It can communicate with the computer over an IEEE 488 bus, Ethernet, serial port, or parallel port.

When there is no choice but to locate an ADC inside the computer, however, check its noise level. Connecting the ADC's input terminal to the signal common terminal should produce an output of zero volts. If it still reads a value when shorted, the noise is being generated on the circuit card and will interfere with the desired input signal. More critical diagnostics are necessary when using an external power supply because noise also can arise from both the power supply and the input leads.

Noise Reduction and Measurement Accuracy

One technique for reducing noise and ensuring measurement accuracy is to eliminate ground loops, that is, current flowing in the ground connection between different devices. Ground loops often occur when two or more devices in a system, such as a measurement instrument and a transducer, are connected

to ground terminals at different physical locations. Slight differences in the actual potential of each ground point generate a current flow from one device to the other. This current, which often flows through the low potential lead of a pair of measurement wires generates a voltage drop that appears as noise and measurement inaccuracy at the signal conditioner or ADC input. When at least one device can be isolated, such as the transducer, then the offending ground path is open, no current flows, and the noise or inaccuracy is eliminated. Optical isolators, special transformers, and differential input operational amplifiers at the signal conditioner or ADC input can provide this isolation.

ADC NOISE HISTOGRAMS

ADC manufacturers frequently verify their device's accuracy (effect of non-linearities) by running a code density test. They apply a highly accurate sine wave signal (precision amplitude and frequency) to the device and using a histogram for analysis, generate a distribution of digital codes at the output of the converter. A perfect ADC would produce only one vertical bar in the histogram for the specified input frequency and amplitude because it measured only one value for every sample. But because of the ADC's inherent non-linearities, it produces a distribution of bars on either side representing digital words sorted into different code bins. Each bin is labeled for a single digital output code and it contains the count of its occurrence, or the number of times that code showed up in the output. (See Figure 2.08.)

When n represents the ADC's bit resolution, 2^n bins are required. The width of each code bin should be $FSR/2^n$ where FSR is the full-scale range of the ADC. The probability density function may be determined from this data. A large number of samples must be taken, depending on the ADC's bit size, for the histogram test to be meaningful. The more bits the ADC contains, the higher the number of samples required, which could be as much as 500,000 samples.

ENOB: EFFECTIVE NUMBER OF BITS

Although an ADC's accuracy is crucial to a data acquisition system's accuracy, it's not the final word. A widely used and practical way of determining overall measurement accuracy is accomplished with what's called an Effective Number of Bits (ENOB) test. The ENOB may very well demonstrate that the actual system measurement accuracy is something less than the ADC bit accuracy specifications. For example, an ADC may be specified as a 16-bit device, but the results of a specific type of standard test may show that its performance is actually closer to an ideal 13-bit system. However, 13 bits may be more than adequate for the application.

The ENOB test takes into account all the circuitry from input terminals to the data output, which includes the effects of the ADC, multiplexer, and other analog and digital circuits on the measurement accuracy. It also includes the signal-to-noise ratio, SNR, or the effect of any noise signals induced into the system from any source.

The ENOB Test

The ENOB test evaluates the data acquisition system as it performs in a real-world application when used with the manufacturers recommended cables, connectors, and connections. It considers the front end of the data acquisition system: the ADC, multiplexer, programmable gain amplifier, and sample-and-hold amplifiers. All of these circuits affect the digitized output. Any non-linearities, noise, distortion, and other anomalies that sneak into the front end can reduce the system's accuracy, and it's not enough to test only one channel in a multi-channel system. Some errors creep up from the effect of one channel on another through cross talk.

To measure the ENOB, set up a precision sine-wave signal generator and connect its output to the input of one analog input channel. The generator itself should produce little noise and distortion. Set the signal generator output amplitude to just under the maximum specified input range of the board. Set the generator to the maximum frequency that the system is specified to measure. Next, ground the input terminals of the adjacent channel. Run the system at its maximum rated speed. Sample the test signal and then the grounded input. Capture 1024 samples on each input and run the samples through an FFT algorithm to compute the ENOB.

The test measures the effects of slewing, harmonic distortion, analog circuits, ADC accuracy, noise pickup, channel cross talk, integral and differential non-linearity, and offset between

channels. Although ENOB provides a good benchmark of the systems capability and accuracy, it is not a specification; it is not a replacement for SNR and other error specifications provided by the manufacturer. However, systems may be compared with ENOB tests when all are measured under the same set of conditions.

ADC OUTPUT AVERAGING BENEFITS

Improved Accuracy

A paradox that arises from averaging the output of an integrating-type ADC is that the measurement system theoretically can obtain higher accuracy for a signal embedded in noise than a signal free of noise. How this can be true comes from the way a signal is mathematically averaged. For example, with a single DC signal, averaging the output always provides the same result with no apparent change in accuracy (not considering the affects of calibration). But for a varying input signal, such as a sine wave, a large number of samples yield a Gaussian distribution which can be accurately defined with a more precisely established peak for the wave. But the samples must not all cluster around a specific portion of the sampled wave. To get a true distribution, the ADC must sample at a slower rate than the fluctuations and be out of synch with them. This technique finds a general average, not a local average. Thus, in this way signal averaging increases the system's measurement resolution.

More Stable Readings

Some systems actually introduce a random noise signal called dither into an otherwise clean ADC input to take advantage of the averaging function for increasing accuracy and signal stability. The technique also enables an ADC with a smaller number of bits to obtain the resolution of an ADC with more bits without losing accuracy. Each signal sweep must capture a different random value at each point in time. Then the theoretical ADC average from this distribution will remain at zero over a sufficiently large sample window. For example, if 16 values are averaged, then it has 16 times more possible values than the direct non-averaged output. This technique increases the effective ADC resolution by 4 bits. The noise makes it work.

ADC signal averaging is so important a technique that it is used on digital recordings. In the early days of digital audio recording development, systems lacked ADC output averaging. As a result, a musical note would decay into an annoying buzz because not all bits in the ADC were enabled. The output waveforms were distorted and the ear could not filter it out, but ADC signal averaging totally eliminated the problem.

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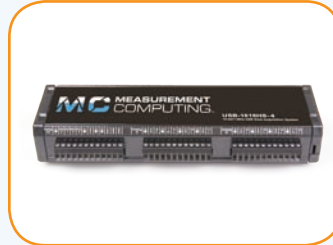
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