CIO-DAS800

User's Guide

Revision 2A
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1 INTRODUCTION

The primary function of the board is to accept up to eight analog voltages and convert them to digital equivalents for transmission to an ISA-bus computer. The inputs circuits are single-ended and accept voltages in a +/-5V range. The board has a resolution of 12 bits (1 in 4096) and a maximum sampling rate of 50 kHz when using the built-in 256-sample FIFO buffer.

The board also contains three 16-bit down-counters.

There are seven bits of digital I/O (3-input, 4-output) that are typically used to control external channel expansion and signal conditioning boards.

2 INSTALLATION

2.1 SOFTWARE INSTALLATION

Before you open your computer and install the board, install and run *Insta*Cal™, the installation, calibration and test utility included with your board. *Insta*Cal™ will guide you through switch and jumper settings for your board. Detailed information regarding these settings can be found below. Please refer to the *Software Installation Manual* for *Insta*Cal™ installation instructions.

2.2 HARDWARE INSTALLATION

The CIO-DAS800 board is an extension of the popular CIO-DAS08 architecture. The CIO-DAS800 has a set of registers identical to the CIO-DAS08, and an additional set of registers for the extended functions. Software written for the DAS08 will work without modification, but will not provide access to the extended functions. The connector is nearly identical to the CIO-DAS08. There are two jumpers and a switch that should be set before installing the CIO-DAS800 into your computer.

2.2.1 BASE ADDRESS

The base address of the CIO-DAS800 is set by switching a bank of DIP switches on the board. This bank of switches is labeled ADDRESS and numbered 9 to 3.

Ignore the word ON and the numbers printed on the switch

The switch works by adding up the weights of individual switches to make a base address. A 'weight' is active when the switch is down. As shown in Figure 2-1, switches 9 and 8 are down, all others are up.

Weights 200h and 100h are active, totalling a 300h base address. Table 2-1 lists PC I/O addresses and their uses.

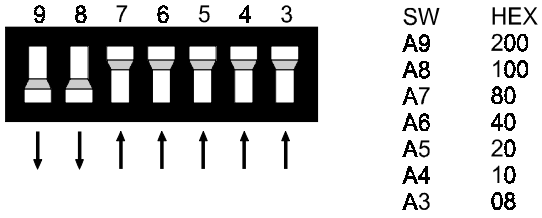

Figure 2-1. Base Address Switches

Table 2-1. PC I/O Addresses

HEX RANGE	FUNCTION	HEX RANGE	FUNCTION
000-00F	8237 DMA #1	2C0-2CF	EGA
020-021	8259 PIC #1	2D0-2DF	EGA
040-043	8253 TIMER	2E0-2E7	GPIB (AT)
060-063	8255 PPI (XT)	2E8-2EF	SERIAL PORT
060-064	8742 CONTROLLER (AT)	2F8-2FF	SERIAL PORT
070-071	CMOS RAM & NMI MASK (AT)	300-30F	PROTOTYPE CARD
080-08F	DMA PAGE REGISTERS	310-31F	PROTOTTYPE CARD
0A0-0A1	8259 PIC #2 (AT)	320-32F	HARD DISK (XT)
0A0-0AF	NMI MASK (XT)	378-37F	PARALLEL PRINTER
0C0-0DF	8237 #2 (AT)	380-38F	SDLC
0F0-0FF	80287 NUMERIC CO-P (AT)	3A0-3AF	SDLC
1F0-1FF	HARD DISK (AT)	3B0-3BB	MDA
200-20F	GAME CONTROL	3BC-3BF	PARALLEL PRINTER
210-21F	EXPANSION UNIT (XT)	3C0-3CF	EGA
238-23B	BUS MOUSE	3D0-3DF	CGA
23C-23F	ALT BUS MOUSE	3E8-3EF	SERIAL PORT
270-27F	PARALLEL PRINTER	3F0-3F7	FLOPPY DISK
2B0-2BF	EGA	3F8-3FF	SERIAL PORT

2.2.2 INTERRUPT LEVEL SELECT

The interrupt jumper need only be set if the software you are using requires it. The Universal Library and other programs which take advantage of the REP-INSW high speed transfer capability of the board require an interrupt. If you do set the interrupt jumper, please check your PC's current configuration for interrupt conflicts.

There is a jumper block on the CIO-DAS800 located just above the PC bus interface (gold pins). The factory default setting is that no interrupt level is set. The jumper is in the 'X' position at the factory. It is shown in Figure 2-2 set for IRQ 5.

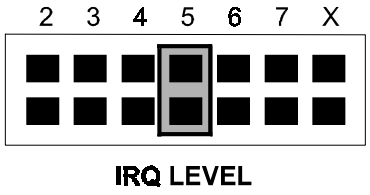

Figure 2-2. IRQ Jumper Block

Table 2-2 lists typical interrupt assignments.

Table 2-2. Typical IRQ Assignments

NAME	DESCRIPTION	NAME	DESCRIPTION
NMI	PARITY	IRQ8	REAL TIME CLOCK (AT)
IRQ0	TIMER	IRQ9	RE-DIRECTED TO IRQ2 (AT)
IRQ1	KEYBOARD	IRQ10	UNASSIGNED
IRQ2	RESERVED (XT) INT 8-15 (AT)	IRQ11	UNASSIGNED
IRQ3	COM OR SDLC	IRQ12	UNASSIGNED
IRQ4	COM OR SDLC	IRQ13	80287 NUMERIC CO-P
IRQ5	HARD DISK (XT) LPT (AT)	IRQ14	HARD DISK
IRQ6	FLOPPY DISK	IRQ15	UNASSIGNED
IRQ7	LPT	Note: IRQ8-15 are AT only	

2.2.3 WAIT STATE

A wait state can be enabled on the CIO-DAS800 by selecting WAIT STATE ON at the jumper provided on the board. Enabling the wait state causes the personal computer's bus transfer rate to slow down whenever the CIO-DAS800 is written to or read from. The wait state jumper is provided in case you one day own a personal computer with an I/O bus transfer rate which is too fast for the CIO-DAS800. If your board fails sporadically in random ways, try setting the wait state ON.

2.2.4 INSTALLING THE CIO-DAS800 IN THE COMPUTER

1. Turn the power off.
2. Remove the cover of your computer. Please be careful not to dislodge any of the cables installed on the boards in your computer as you slide the cover off.
3. Locate an empty expansion slot in your computer.
4. Push the board firmly down into the expansion bus connector. If it is not seated fully it may fail to work and could short circuit the PC bus power onto a PC bus signal. This could damage the motherboard in your PC as well as the board.
5. Power up your computer and run the *Insta*Cal test to verify your hardware installation.

3 CONNECTOR DIAGRAM

The CIO-DAS800 analog connector is a 37-pin, D-type connector accessible from the rear of the PC through the expansion backplate (Figure 3-1). The connector accepts female 37-pin D-type connectors, such as those on the C37FF-2, a 2-foot cable with connectors.

If frequent changes to signal connections or signal conditioning is required, please refer to the information on the CIO-TERMINAL and CIO-MINI37 screw terminal boards, CIO-EXP32, 32 channel analog MUX/AMP. Isolation amplifiers can be mounted using the ISO-RACK08 and 5B isolation modules.

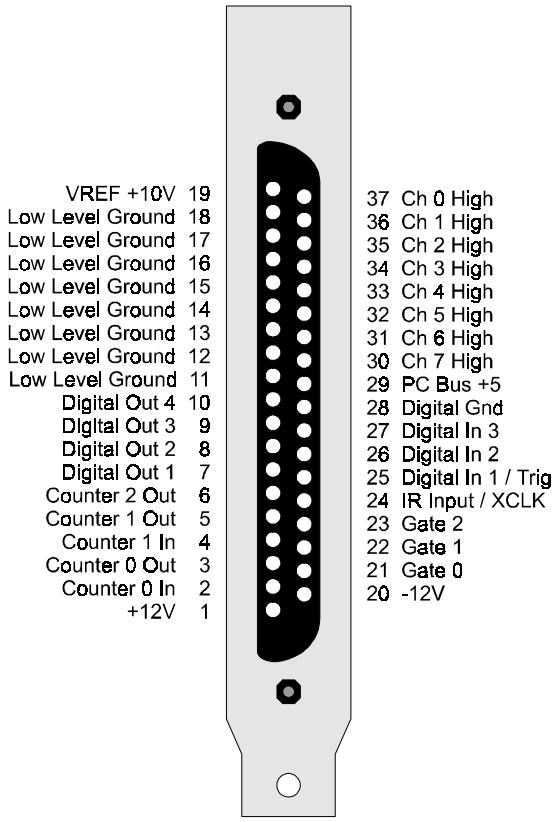

Figure 3-1. Analog Connector

WARNING - PLEASE READ

Measure the voltage between the ground signal at the signal source and the PC. Use a high input impedance voltmeter. If there more the 10 volts, do not connect the CIO-DAS800 to this signal source because you will not be able to make a reading. If the difference is more than 30 volts, DO NOT connect this signal to the CIO-DAS800 because IT WILL DAMAGE the board and possibly the computer.

4 OPERATIONAL ASPECTS - CIO-DAS800 VS. CIO-DAS08

4.1 CONVERSION TRIGGER

A trigger is the event that begins an acquisition/transfer cycle. There are three ways to trigger a CIO-DAS800; software, interrupt service routine or hardware. The hardware trigger is a new feature on the CIO-DAS800, not found on the other DAS08 family boards. This new, improved trigger allows the board to run much faster than the other DAS08 boards.

Briefly, there are three methods to trigger a data conversion:

A software trigger starts an A/D conversion when an addressed port is written to. This is how a single sample may be taken.

An interrupt service routine is a set of instructions executed by the computer when an interrupt is received. The source of the interrupt is the IR input pin. The signal on the IR input pin is routed to the PC bus via the interrupt jumper on the CIO-DAS800. The event that causes the interrupt may be the internal 82C54 counter or an external event.

The hardware trigger is a direct input to the A/D chip's start conversion pin. When the trigger is received, the A/D starts a conversion. When the conversion is complete, the data is transferred to the FIFO buffer. The source for the hardware trigger can be the 82C54 counter/pacer or an external event.

A trigger is useful for synchronizing samples to a known time base, such as the on board 82C54 programmable divider. Using an external trigger allows you to synchronize samples to an external event.

4.2 IMPROVED CHANNEL SEQUENCER

When the acquisition strategy you set up requires a scan of data from multiple channels, the channel sequencer controls the internal multiplexer that routes the signal to the A/D. The DAS08 family employs a register that must be written to each time the mux is incremented.

The improved hardware channel sequencer on the CIO-DAS800 is set up, then takes over control of the internal multiplexer, freeing the CPU from that task. This gives faster sampling.

4.3 CONTROL REGISTERS

The CIO-DAS800 is compatible with DAS08 software because the basic I/O register have identical functions on each board. I/O registers are the locations which the computer writes commands and data to and reads status and data from. Table 1-1 is a summary of board registers. The register at BASE+2 is a multi-function register. It and the others are described in the register section of this manual.

Table 1-1. Register Summary

I/O ADDRESS	FUNCTION Read/ Write
BASE + 0	A/D Low Byte / Start Conv A/D
BASE + 1	A/D High Byte / Start Conv A/D
BASE + 2	Special Multi-Functions Register
BASE + 3	Gain & Range Control / Status

BASE + 4	Read Counter 0/ Load Counter 0
BASE + 5	Read Counter 1 / Load Counter 1
BASE + 6	Read Counter 2 / Load Counter 2
BASE + 7	Status & ID / Counter Control

4.4 FIFO

The FIFO buffer is 256 bytes deep. A larger FIFO makes higher throughput of A/D conversions possible. This is important when running Windows, and will be more important in future versions of that OS. This does not affect compatibility in any way because it is a hardware-only function and is transparent to the software.

4.5 FIFO HALF-FULL INTERRUPT

In addition to a larger FIFO, the CIO-DAS800 has a 1/2-full interrupt. This means that a transfer request is made after the CIO-DAS800 accumulates 128 samples instead of after every sample. This greatly improves throughput. This does not affect compatibility with other similar boards in any way because it is a hardware function and is transparent to the software.

4.6 WAIT STATE JUMPER

Adding this jumper causes a wait state to be inserted into each CPU cycle whenever the CIO-DAS800 is accessed. This may be necessary on machines with very fast ISA busses, but the need for the wait state is very rare. This jumper does not affect compatibility in any way because it is a hardware function and is transparent to the software.

4.7 REFERENCE VOLTAGE

The CIO-DAS800 A/D converter, an AD674, provides a precision 10V reference.

4.8 SINGLE-ENDED ANALOG INPUTS

The board accepts single-ended inputs only. Each input has two wires connected to the CIO-DAS800; a channel high (CH# HI) and a Low Level Ground (LLGND). The LLGND signal *must be the same ground the PC is on.* The CH# HI is the voltage signal source in the range of +/-5V maximum.

4.9 DIGITAL OUTPUTS & INPUTS

The digital inputs and outputs on the CIO-DAS800 are TTL level. TTL is an electronics industry term, short for Transistor Transistor Logic, which describes a standard for digital signals. For a listing of the TTL level specifications for these digital lines, please see the specifications at the end of this manual.

There are three digital inputs and four digital outputs. The digital outputs are controlled by a register on the board and are updated each time the register is written to. The digital inputs are buffered by a register on the board. Each time the register is read, the current high/low state of the digital I/O lines is obtained. The lines are pulled high so a one (1) is read when no signal is connected to an input

Typically, the digital lines are used to control external expansion boards (all four outputs) and to trigger and gate A/D conversions (IP0 input).

4.10 COUNTER TIMER CIRCUIT

There is an 82C54 counter/timer on the board which can be used to:

- Pace analog conversions
- Measure frequency
- Count events
- Precisely time intervals

The Universal Library has software to support the timer. The connections to the hardware are explained here. For detailed information on the 82C54 registers, please refer to the Intel or AMD data sheet for this part if you wish to program the 82C54 registers directly.

The 82C54 contains three counters, each is 16 bits wide. Of the three counters, two are dedicated to pacing analo-to-digital conversions. These two, CTR1 and CTR2, when not in use by the A/D, are available for other tasks but are limited to some extent by access to I/O pins. The first counter, CTR0, is available for user applications.

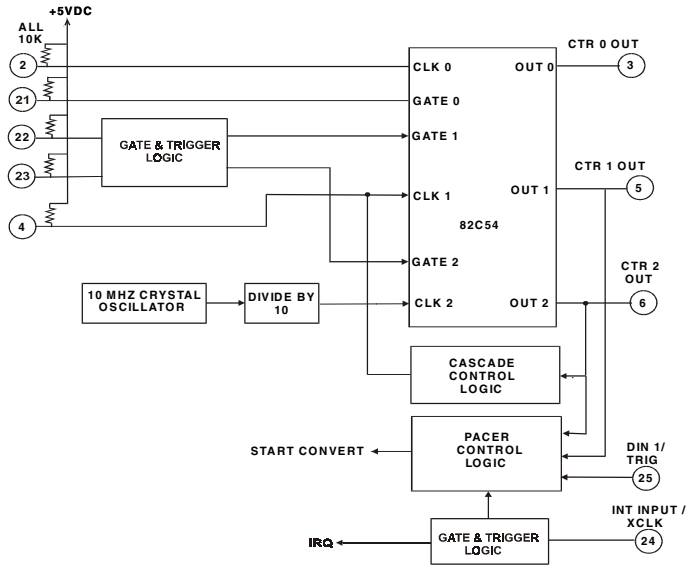

Figure 1-1. Counter/Timer Functional Diagram

Figure 1-1 shows the 82C54 functions, I/O pins and how these are connected on the CIO-DAS800.

The CIO-DAS800 CTR2 input is connected to the PC bus clock/2 or the 1 MHz. crystal signal. The system default is the PC bus clock.

Software controls the counters that generate the A/D pacing pulse.

Note: A/D conversions are triggered by falling-edge signals. The pulses generated by the 82C54 are low-going for one count length. The A/D is triggered as the signal goes low. Any A/D trigger signal you supply externally must also be low-going at the desired moment of A/D conversion.

5 REGISTER MAP

Tables 4-1 and 4-2 contain the write and read functions of the board's registers. Table 4-3 defines the functions of each bit.

Note that the register at BASE + 2 is a multi-function register. Its function is set by bits CS0 and CS1 in BASE + 3 register. Coding for Base + 02 register functions is contained in Table 4-4.

Table 4-5 gives the Gain Select codes for the CIO-DAS800.
NOTE: ONLY +/-5V IS SUPPORTED.

Table 4-6 provides special programming instructions.

Table 4-1. Register Map - Write Functions

WRITE Functions				**Data Bits**					**Function**
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Base + 0									Start Conversion*
Base + 1									Start Conversion*
Base + 2			***Special Function - (Depends on value of CS0,1)***						
CS1/0=0/0	OP4	OP3	OP2	OP1	INTE	MA2	MA1	MA0	Control Register 1
CS1/0=0/1	HCEN	NA	GTEN	EACS	IEOC	DTEN	CASC	ITE	Conversion Control
CS1/0=1/0	NA	NA	EC2	EC1	EC0	SC2	SC1	SC0	Scan Limits Register
Base + 3	CSE	CS1	CS0	ENHF	R3	R2	R1	R0	Control Select
Base + 4			8254 C/T 0 Control Register						
Base + 5			8254 C/T 1 Control Register						A/D Timer
Base + 6			8254 C/T 2 Control Register						Cascade Pre-scaler
Base + 7			8254 Counter/Timer Control Register						Register

* Writing (anything) to either BASE + 0 or BASE + 1 starts a conversion.

Table 4-2. Register Map - Read Functions

READ Functions				**Data Bits**					**Function**	
Register	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
Base + 0	AD3	AD2	AD1	AD0	FF3	FF2	FFOV	FFEM	Low byte read	
Base + 1	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	High byte read	
Base + 2	EOC	IP3	IP2	IP1	IRQ	MA2	MA1	MA0	Status Register 1	
Base + 3	EACS	MA2	MA1	MA0	R3	R2	R1	R0	Control Status	
Base + 4			8254 C/T 0 Status Register							
Base + 5			8254 C/T 1 Status Register							
Base + 6			8254 C/T 2 Status Register							
Base + 7			***Function depends on value of CS0/1 bits in Base +3:***							
CS1/0= 0/0,0/1,1/0	HCEN	GTEN	INTE	IEOC	DT	DTEN	CASC	ITE	Status Register 2	
CS1/0 = 1/1	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	ID Reg (ID1,0 = 0/0)	

Table 4-3. Bit Definitions

DEFINITIONS:										
AD 11:0	*R*	Analog data input (Read low byte first)								
MA2:0	*RW*	Mux address bits								
INTE	*RW*	Interrupt enable (0 = disable, 1 = enable)								
EOC	*R*	End-of-conversion (1 = busy, 0 = ready)								
HCEN	*RW*	Hardware Convert Enable								
GTEN*	*RW*	Gate Enable (Req. DTEN to enable HW gate)								
EACS*	*RW*	Enable Auto channel-scan								
IEOC	*RW*	Interrupt Source (1 = End of Convert, 0 = Ext)								
DTEN*	*RW*	External Digital Trigger Enable (Edge trig if GTEN=0)								
CASC*	*RW*	Cascade AD Pacing Mode Enable (include CT/2)								
ITE*	*RW*	Internal Time Base (8254) Enable								
CSE	*W*	Register Select Enable/Range Select Disable								
CS1:0	*W*	Register Selection (See Table Below)								
R3:0	*RW*	(N/A)								
ENHF*	*W*	Enable Interrupt on FIFO Half Full (Req. IEOC=1, HCEN must =1 to enable FIFO)								
DT*	*R*	State of Digital Trigger (1=Trigger occured)								
FFEM*	*R*	FIFO Empty =1. 0 if HCEN =0.								
FFOV*	*R*	FIFO Overflow (full) =1. 0 if HCEN =0.								
FF2*	*R*	0 if HCEN =0. 0 if HCEN =1 & FIFO not empty. Undefined if HCEN = 1 and FIFO empty								
FF3*	*R*	0 if HCEN =0. 0 if HCEN =1 & FIFO not empty. Undefined if HCEN = 1 and FIFO empty								
SC2:0*	*W*	Channel-scan start value.								
EC2:0*	*W*	Channel-scan end value								
IP3:1	*R*	Digital Input bits.								
OP4:1	*W*	Digital Output bits.								
		*** Asterisk indicates that HCEN is required (as a final step) to make this bit functional.**								

Table 4-4. Coding for Base + 02 Register Functions

Control Register Selected			
CS1	CS0	Write Function	Read Function
0	0	Control Reg # 1	Status Register #2
0	1	Conversion Control	Status Register #2
1	0	Scan Limits Reg	Status Register #2
1	1	Not defined	ID Register

Table 4-5. Special Programming Instructions

Special Programming instructions					
Register					
Conv/Control	HCEN is used as a master enable for AD Pacing				
	Set HCEN last, by itself (ie write 80h) , set the other bits first				
Scan Limits	Ending channel (n) can be lower than starting channel (m) : m,...,6,7,0,1,...,n,m...				
	Select Start and End Channel before setting EACS				
ID	Only the 1st two bits are needed for software, the upper six are for compatibility with KMB software				
	ID 1/0: 0/0= (DAS800], 0/1= reserved, 1/0= N/A, 1/1= N/A)				
Gain/Range	Not appplicable.				
Operating modes					
Pacing	Normal	CT/2 divides the 1MHz timebase; AD converts when CT/2 counts to zero			
	Cascade	CT/1 decrements each time CT/2 counts to zero; AD converts when CT/1 counts to zero			
Triggering	Edge	Requires DTEN=1, GTEN=0			
Gating	Level	"Gate", Requires DTEN=1, GTEN=0			
Bit					
INT/XCLK	External Interrupt and External (Pacer) Clock are mutually exclusive				
	External Interrupt is rising edge, External Pacer is falling edge				

6 SPECIFICATIONS

Power consumption

+5V quiescent	450 mA typical, 600 mA max

Analog input section

A/D converter type	AD674A, Successive Approximation
Resolution	12 bits
Number of channels	8
Input Ranges	±5V fixed
Polarity	Bipolar fixed
A/D pacing	Programmable: internal counter or external source (IR Input / XCLK, falling edge) or software polled
A/D Trigger sources	External hardware (Digital In 1 / Trig, rising edge)
Data transfer	Interrupt or software polled from 256 sample FIFO buffer
Channel configuration	Single-ended
DMA	None
A/D conversion time	20 µs
Throughput	50 kHz
Accuracy	±0.01% of full scale ±1 LSB typ, ±0.05% of full scale ±1 LSB max
Differential Linearity error	±0.5 LSB max
Integral Linearity error	±1 LSB
No missing codes (guaranteed)	12 bits
Gain drift (A/D specs)	±50 ppm/°C
Zero drift (A/D specs)	±10 ppm/°C
Common Mode Range	±10V
CMRR @ 60 Hz	70 dB min
Input leakage current (@ 25 deg C)	± 30 nA
Input leakage current (over temperature)	±250 nA
Input impedance	>1000 Mohm typical
Absolute maximum input voltage	±35V

Counter section

Counter type	82C54
Configuration	3 down-counters , 16 bit resolution
	Counter 0 - independent user counter
	Source: external, user connector (Counter 0 In)
	Gate: external, user connector (Gate 0)
	Output: user connector (Counter 0 Out)
	Counter 1 - ADC Pacer Lower Divider or independent user counter
	Source: user connector (Counter 1 In) and optionally, Counter 2 Out, selectable by software
	Gate: Programmable, disabled or user connector (Gate 1)
	Output: User connector (Counter 1 Out) and optionally to A/D start convert, software selectable
	Counter 2 - ADC Pacer Upper Divider
	Source: Internal 1 MHz oscillator
	Gate: Programmable, disabled or user connector (Gate 2)
	Output: User connector (Counter 2 Out) and optionally to counter 1 input, software selectable
Clock input frequency	10 MHz max
High pulse width (clock input)	30 ns min
Low pulse width (clock input)	50 ns min
Gate width high	50 ns min
Gate width low	50 ns min
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage	0.4V max
Output high voltage	3.0V min
Crystal oscillator	
Frequency	1 MHz
Frequency accuracy	100 ppm

Digital I/O section

Digital type	FPGA
Configuration	Two ports, 3 input and 4 output
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage (IOL = 4 mA)	0.32V max
Output high voltage (IOH = –4 mA)	3.86V min
Absolute maximum input voltage	–0.5V , +5.5V

Interrupts	Jumper selectable: levels 2, 3, 4, 5, 6, 7 or not connected
	Positive-edge triggered
Interrupt enable:	Programmable
Interrupt sources:	External (IR Input / XCLK), A/D End-of-conversion, A/D FIFO Half-Full

Environmental

Operating temperature range	0 to 50°C
Storage temperature range	–20 to 70°C
Humidity	0 to 90% non-condensing

EC Declaration of Conformity

We, Measurement Computing Corp., declare under sole responsibility that the product:

CIO-DAS800	Analog input board with counters and digital I/O
Part Number	Description

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

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