USB-1808

Eight-Channel Simultaneous-Sampling Multifunction Device

User's Guide

MEASUREMENT COMPUTING™

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Table of Contents

About this User's Guide

What you will learn from this user's guide

This user's guide describes the Measurement Computing USB-1808 data acquisition device and lists device specifications.

Conventions in this user's guide

For more information

Text presented in a box signifies additional information and helpful hints related to the subject matter you are reading.

Caution! Shaded caution statements present information to help you avoid injuring yourself and others, damaging your hardware, or losing your data.

Bold text is used for the names of objects on a screen, such as buttons, text boxes, and checkboxes.

Italic text is used for the names of manuals and help topic titles, and to emphasize a word or phrase.

Where to find more information

Additional information about USB-1808 hardware is available on our website at www.mccdaq.com. You can also contact Measurement Computing Corporation with specific questions.

- Knowledgebase: kb.mccdaq.com
- Tech support form: www.mccdaq.com/support/support_form.aspx
- Email: techsupport@mccdaq.com
- Phone: 508-946-5100 and follow the instructions for reaching Tech Support

For international customers, contact your local distributor. Refer to the International Distributors section on our web site at www.mccdaq.com/International.

Introducing the USB-1808

The USB-1808 is a multifunction data acquisition device providing the following features:

- Eight 18-bit simultaneous-sampling differential (DIFF) or single-ended (SE) analog input channels – software-selectable per channel as DIFF or SE
- Sample rate of 50 kS/s per channel maximum
- Analog input ranges of ±10 V, ±5 V, 0 V to 10 V, and 0 V to 5 V – software-selectable per channel
- Two 16-bit analog outputs
- Four individually-configurable digital I/O channels
- Two high-speed general-purpose counters
- Two quadrature encoder inputs
- Two timer outputs
- One external digital trigger for data acquisition and one external digital trigger for data generation
- Two external clock inputs and two clock outputs for synchronous input and output operations with more than one device.
- Screw terminals for field wiring connections

The device is powered by the +5 V USB supply from the computer, requiring no external power.

The USB-1808 is a USB 2.0 high-speed device that is fully compatible with both USB 1.1, USB 2.0, and USB 3.0 ports.

Functional block diagram

USB-1808 functions are illustrated in the block diagram shown here.
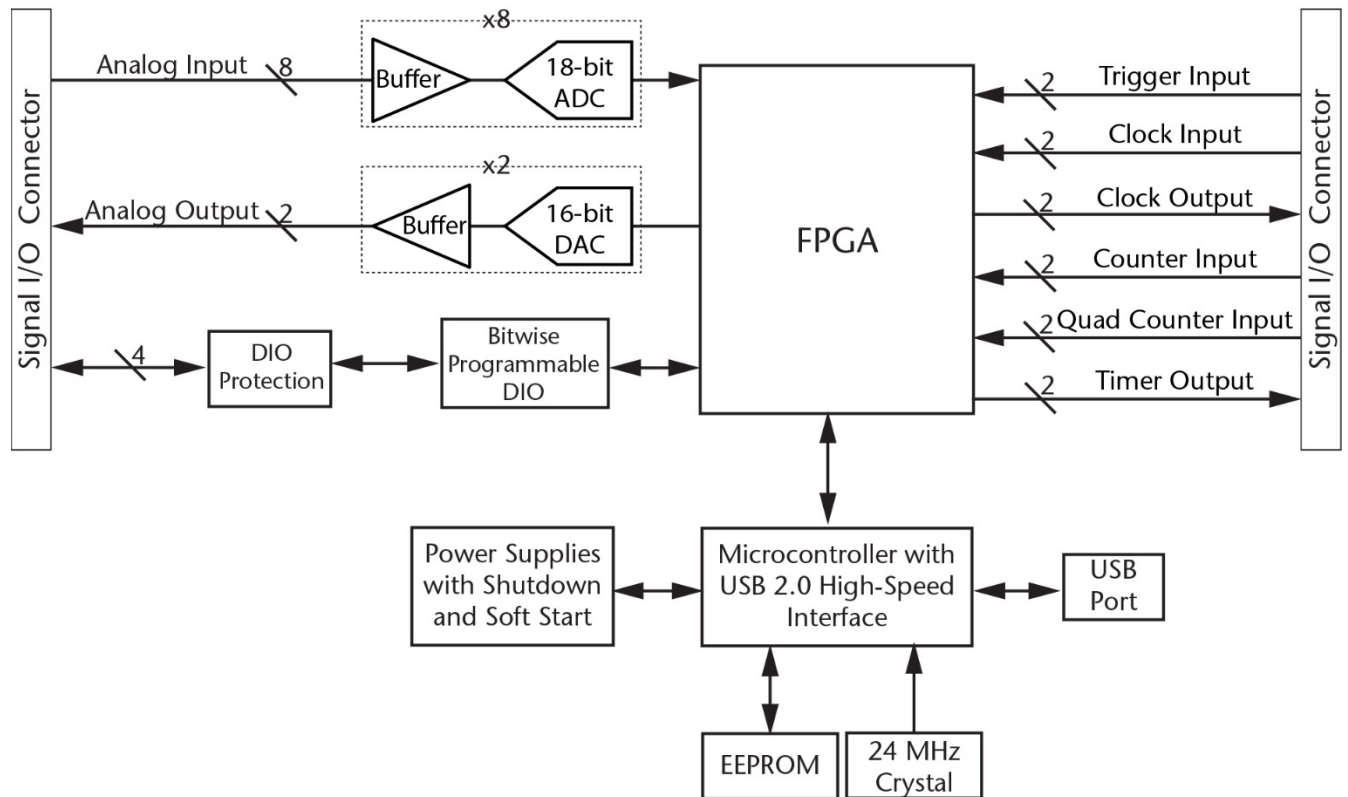
Figure 1. Functional block diagram

Installing the USB-1808

Unpacking

As with any electronic device, you should take care while handling to avoid damage from static electricity. Before removing the device from its packaging, ground yourself using a wrist strap or by simply touching the computer chassis or other grounded object to eliminate any stored static charge.

Contact us immediately if any components are missing or damaged.

Installing the software

Refer to the *MCC DAQ Quick Start* and the USB-1808 product page on our website for information about the software supported by the USB-1808.

Install the software before you install your device

The driver needed to run the USB-1808 is installed with the software. Therefore, you need to install the software package you plan to use before you install the hardware.

Installing the hardware

To connect the USB-1808 to your system, connect the USB cable to an available USB port on the computer or to an external USB hub connected to the computer. Connect the other end of the USB cable to the USB connector on the device. No external power is required.

When connected for the first time, a **Found New Hardware** dialog opens when the operating system detects the device. When the dialog closes, the installation is complete. The **Status** LED on the USB-1808 turns on after the device is successfully installed.

If the Status LED turns off

If communication is lost between the device and the computer, the device LED turns off. To restore communication, disconnect the USB cable from the computer and then reconnect it. This should restore communication, and the LED should turn on.

Calibrating the hardware

The Measurement Computing Manufacturing Test department performs the initial factory calibration. Return the device to Measurement Computing Corporation when calibration is required. The recommended calibration interval is one year.

Updating firmware

Your DAQ device contains firmware that can be updated in the field if required. Firmware is available for download at www.mccdaq.com/firmware.aspx. MCC recommends that you check this page periodically to see if an update to your device firmware is available.

Functional Details

External components

The USB-1808 has the following external components (see Figure 2 through Figure 4 on pgs. 9-10):

- USB connector
- LEDs
- Screw terminals

USB connector

The USB connector provides +5 V power and communication. No external power supply is required.

Screw terminals

The screw terminals provide the following connections:

- Eight DIFF analog inputs (**CH0H/CH0L** to **CH7H/CH7L**) or eight SE analog inputs (**CH0H** to **CH7H**)
  Refer to Figure 2 and Figure 3 on page 9 for DIFF and SE pinouts.
- Two analog outputs (**AOUT0** and **AOUT1**)
- Four digital I/O lines (**DIO0** to **DIO3**)
- Two general-purpose counter inputs (**CTR0** and **CTR1**)
- Two quadrature encoder inputs (**ENC0A**, **ENC0B**, **ENC0Z** and **ENC1A**, **ENC1B**, **ENC1Z**)
- Two timer outputs (**TMR0** and **TMR1**)
- An external trigger input (**ITRIG)** and an external trigger output **OTRIG**)
- Two external clock inputs (**ICLKI** and **OCLKI**) and two external clock outputs (**ICLKO**, **OCLKO**)
- One +5 V power output (**+VO**) connection
- Ten analog ground (**AGND**) and seven digital ground (**GND**) connections

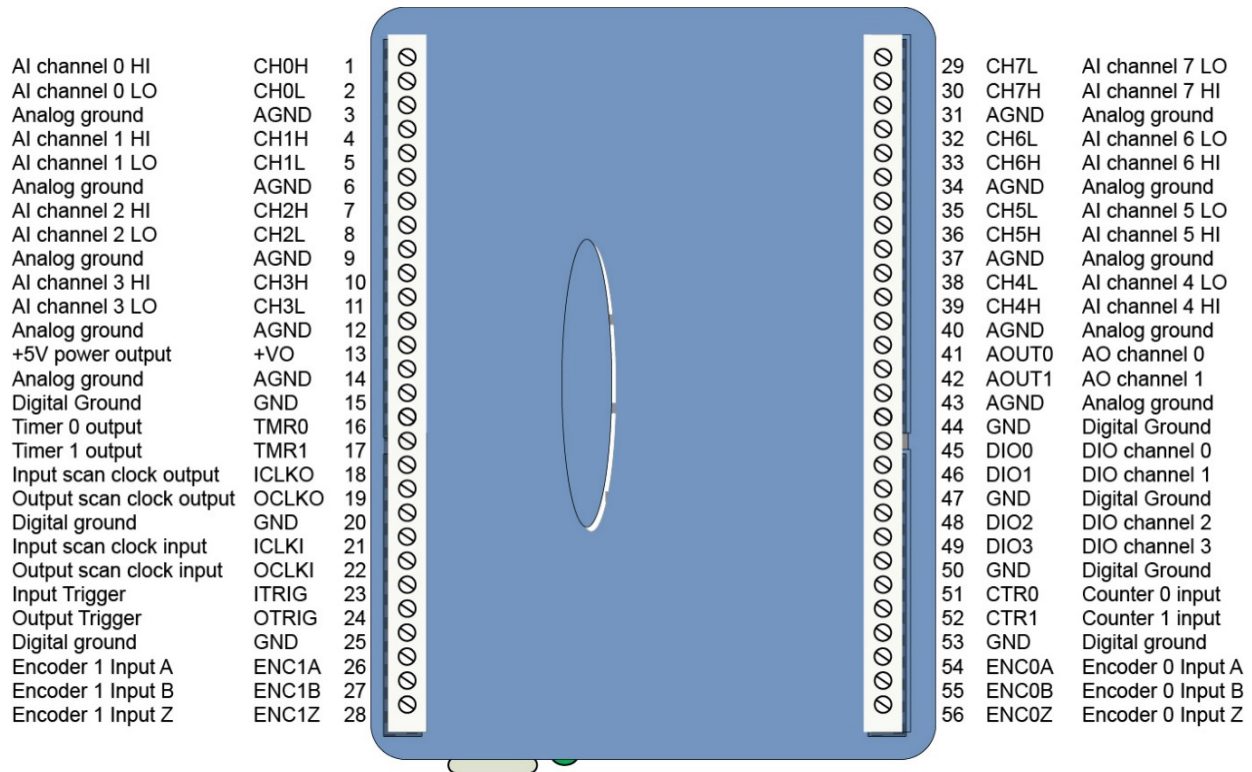Use 16 AWG to 30 AWG wire when making connections to the screw terminals.

AI channel 0 HI	CH0H	1
AI channel 0 LO	CH0L	2
Analog ground	AGND	3
AI channel 1 HI	CH1H	4
AI channel 1 LO	CH1L	5
Analog ground	AGND	6
AI channel 2 HI	CH2H	7
AI channel 2 LO	CH2L	8
Analog ground	AGND	9
AI channel 3 HI	CH3H	10
AI channel 3 LO	CH3L	11
Analog ground	AGND	12
+5V power output	+VO	13
Analog ground	AGND	14
Digital Ground	GND	15
Timer 0 output	TMR0	16
Timer 1 output	TMR1	17
Input scan clock output	ICLKO	18
Output scan clock output	OCLKO	19
Digital ground	GND	20
Input scan clock input	ICLKI	21
Output scan clock input	OCLKI	22
Input Trigger	ITRIG	23
Output Trigger	OTRIG	24
Digital ground	GND	25
Encoder 1 Input A	ENC1A	26
Encoder 1 Input B	ENC1B	27
Encoder 1 Input Z	ENC1Z	28

29	CH7L	AI channel 7 LO
30	CH7H	AI channel 7 HI
31	AGND	Analog ground
32	CH6L	AI channel 6 LO
33	CH6H	AI channel 6 HI
34	AGND	Analog ground
35	CH5L	AI channel 5 LO
36	CH5H	AI channel 5 HI
37	AGND	Analog ground
38	CH4L	AI channel 4 LO
39	CH4H	AI channel 4 HI
40	AGND	Analog ground
41	AOUT0	AO channel 0
42	AOUT1	AO channel 1
43	AGND	Analog ground
44	GND	Digital Ground
45	DIO0	DIO channel 0
46	DIO1	DIO channel 1
47	GND	Digital Ground
48	DIO2	DIO channel 2
49	DIO3	DIO channel 3
50	GND	Digital Ground
51	CTR0	Counter 0 input
52	CTR1	Counter 1 input
53	GND	Digital ground
54	ENC0A	Encoder 0 Input A
55	ENC0B	Encoder 0 Input B
56	ENC0Z	Encoder 0 Input Z

Figure 2. DIFF mode pinout

AI channel 0 HI	CH0H	1
No connection	NC	2
Analog ground	AGND	3
AI channel 1 HI	CH1H	4
No connection	NC	5
Analog ground	AGND	6
AI channel 2 HI	CH2H	7
No connection	NC	8
Analog ground	AGND	9
AI channel 3 HI	CH3H	10
No connection	NC	11
Analog ground	AGND	12
+5V power output	+VO	13
Analog ground	AGND	14
Digital Ground	GND	15
Timer 0 output	TMR0	16
Timer 1 output	TMR1	17
Input scan clock output	ICLKO	18
Output scan clock output	OCLKO	19
Digital ground	GND	20
Input scan clock input	ICLKI	21
Output scan clock input	OCLKI	22
Input Trigger	ITRIG	23
Output Trigger	OTRIG	24
Digital ground	GND	25
Encoder 1 Input A	ENC1A	26
Encoder 1 Input B	ENC1B	27
Encoder 1 Input Z	ENC1Z	28

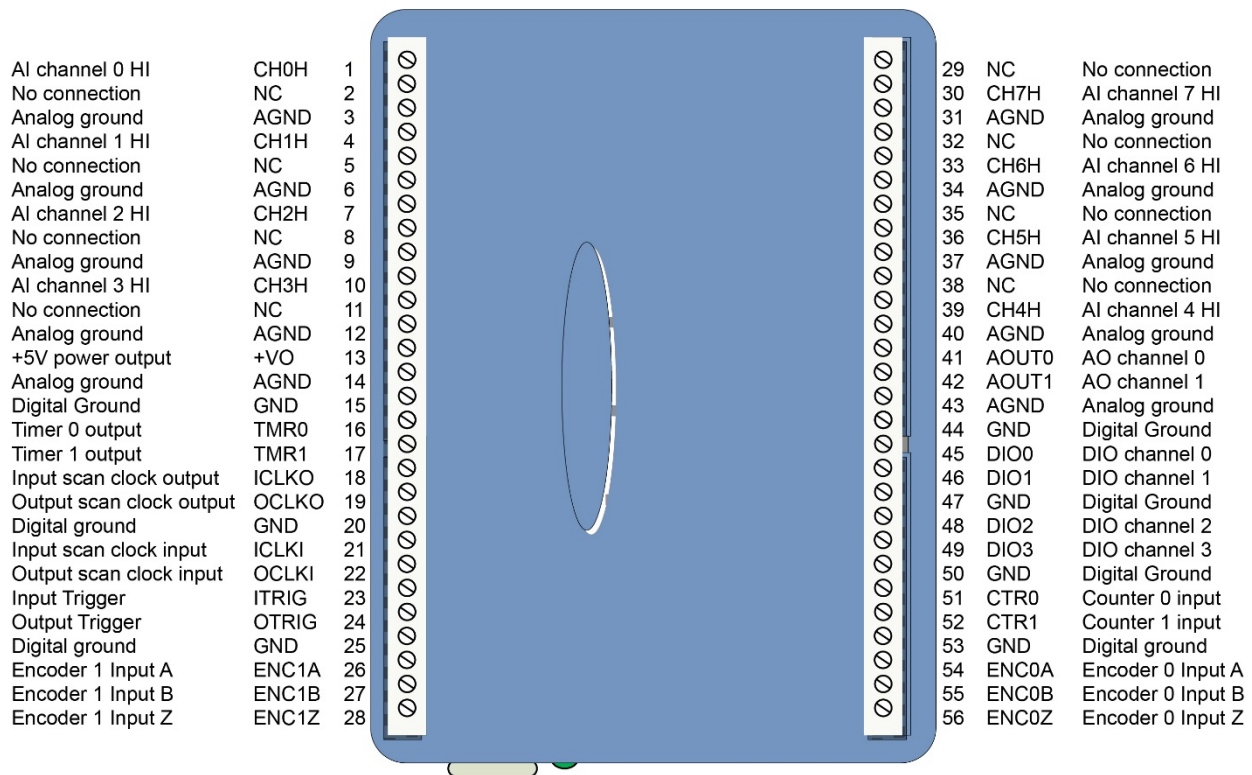| 29	NC	No connection
30	CH7H	AI channel 7 HI
31	AGND	Analog ground
32	NC	No connection
33	CH6H	AI channel 6 HI
34	AGND	Analog ground
35	NC	No connection
36	CH5H	AI channel 5 HI
37	AGND	Analog ground
38	NC	No connection
39	CH4H	AI channel 4 HI
40	AGND	Analog ground
41	AOUT0	AO channel 0
42	AOUT1	AO channel 1
43	AGND	Analog ground
44	GND	Digital Ground
45	DIO0	DIO channel 0
46	DIO1	DIO channel 1
47	GND	Digital Ground
48	DIO2	DIO channel 2
49	DIO3	DIO channel 3
50	GND	Digital Ground
51	CTR0	Counter 0 input
52	CTR1	Counter 1 input
53	GND	Digital ground
54	ENC0A	Encoder 0 Input A
55	ENC0B	Encoder 0 Input B
56	ENC0Z	Encoder 0 Input Z

Figure 3. SE mode pinout

LEDs

The USB-1808 has two LED indicators that indicate the status of power and data. The LEDs are stacked one above the other, as shown in Figure 4.

- The **Status** LED turns on when the device is detected by the computer.
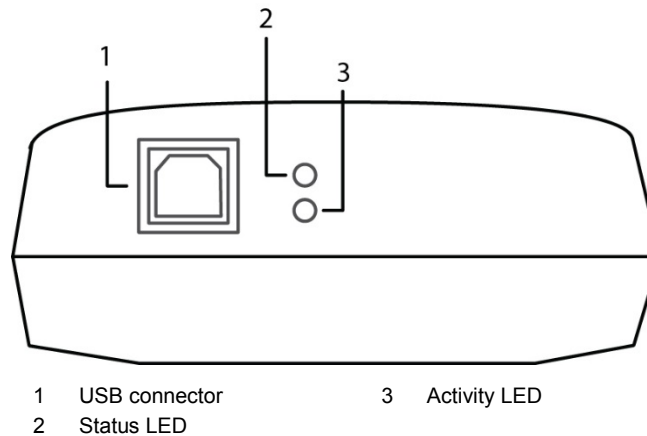- The **Activity** LED blinks when data is transferred and is off otherwise.

1	USB connector	3	Activity LED
2	Status LED		

Figure 4. LED indicators

Analog input

You can configure each analog input channel for either SE or DIFF mode. MCC recommends connecting unused analog input terminals to analog ground terminals during operation. For example, if you are not using **CH7L**, connect this terminal to an available **AGND** terminal.

The input voltage range is software-selectable per channel for ±10 V, ±5 V, 0 V to 10 V, or 0 V to 5 V.

Analog input operations can be paced by the internal clock or by an external clock (**ICLKI** – refer to *Clock I/O* on page 15). They can be initiated by a digital trigger (*Digital triggering* on page 15) or a pattern trigger (*Pattern triggering* on page 15).

Refer to *Synchronous I/O – mixing analog, digital, and counter scanning* on page 15 for information on running analog input scans at the same time as other subsystem scans.

For more information about analog signal connections

For more information about analog input connections, refer to the *Guide to DAQ Signal Connections* (available for download at www.mccdaq.com/support/DAQ-Signal-Connections.aspx).

Channel-Gain queue

The channel-gain queue feature allows you to configure a different gain setting for each channel. The gain settings are stored in a channel-gain queue list that is written to local memory on the device.

The channel-gain queue list can contain up to eight unique elements. The channel list must be in increasing order. An example of a five-element list is shown in the following table.

Sample channel-gain queue list

Element	Channel	Range
0	**CH0H**/**CH0L** (DIFF)	±10 V
1	**CH2H**/**AGND** (SE)	±5 V
2	**CH3H**/**AGND** (SE)	0 V to 5 V
3	**CH6H**/**CH6L** (DIFF)	0 V to 10 V
4	**CH7H**/**CH7L** (DIFF)	±5 V

Carefully match the gain to the expected voltage range on the associated channel or an over range condition may occur. Although this condition does not damage the device, it does produce a useless full-scale reading, and can introduce a long recovery time due to saturation of the input channel.

Analog output

The two 16-bit analog outputs (AOUT0 and AOUT1) can be updated simultaneously at a rate of 250 kS/s per channel. Each output can be updated at a rate of 250 kS/s. The output range is fixed at ±10 V. The outputs default to 0 V at power up, or when a reset command is issued to the device.

Analog output operations can be paced by the internal clock or by an external clock (**OCLKI** – refer to Clock I/O on page 15). They can be initiated by a digital trigger (*Digital triggering* on page 15) or a pattern trigger (*Pattern triggering* on page 15).

Refer to *Synchronous I/O – mixing analog, digital, and counter scanning* on page 15 for information on running analog output scans at the same time as other subsystem scans.

Digital I/O

You can connect up to four digital I/O lines to **DIO0** through **DIO3**. Each digital channel is individually configurable for input or output. During initial power on or reset, the digital pins are set for input.

The digital I/O terminals can detect the state of any TTL-level input. Refer to the schematic shown in Figure 5.
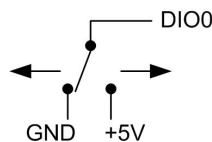

Figure 5. Schematic showing switch detection by digital channel DIO0

If you set the switch to the +5 V input, DIO0 reads TRUE (1). When set to GND, DIO0 reads FALSE (0).

Digital input scanning

Digital input operations can be paced by the internal clock or by an external clock (**ICLKI** – refer to *Clock* I/O on page 15). They can be initiated by a digital trigger (*Digital triggering* on page 15) or a pattern trigger (*Pattern triggering* on page 15).

If no analog inputs are being scanned, the digital inputs can sustain rates up to 200 kHz. Digital input ports can also be read asynchronously before, during, or after an analog input scan.

Refer to *Synchronous I/O – mixing analog, digital, and counter scanning* on page 15 for information on running digital input scans at the same time as other subsystem scans.

Pull-up/down configuration

All digital I/O lines are pulled down to 0 V (LO) with a 47 kΩ resistor (default). You can change the pull-up/down configuration using the internal jumper labeled **DIO**. You must remove the device housing to access the jumper on the circuit board.

To set the jumper for pull-up or pull-down, complete the following steps.

1. Unplug the device from the computer.
2. Turn the device over and rest the top of the housing on a flat, stable surface.

Caution!   The discharge of static electricity can damage some electronic components. Before removing the USB-1808 from its housing, ground yourself using a wrist strap or touch the computer chassis or other grounded object to eliminate any stored static charge.

3. Remove the rubber fee from the bottom of the device, and the four screws using a #1 Philips head screwdriver.

4. Hold both the top and bottom sections together, turn the device over and rest it on the surface, then carefully remove the top section of the case to expose the circuit board.

   Figure 6 shows the location of the **DIO** jumper on the circuit board.
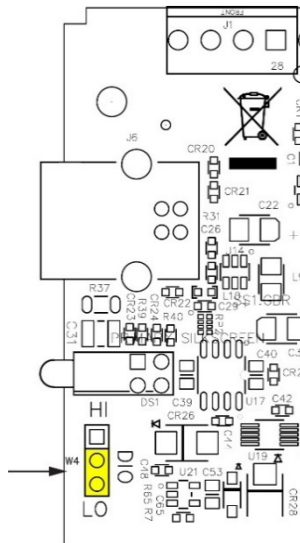

Figure 6. Pull-up/down jumper location

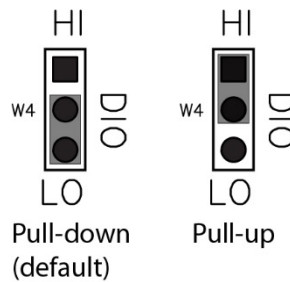5. Configure the **DIO** jumper for pull-up or pull-down, as shown in Figure 7.

Figure 7. Pull-up/down jumper configuration

6. Replace the top section of the housing and fasten it to the bottom section with the four screws.

For more information about digital signal connections

For general information about digital signal connections and digital I/O techniques, refer to the *Guide to DAQ Signal Connections* (available for download at www.mccdaq.com/support/DAQ-Signal-Connections.aspx).

Counter input

Counter inputs can be read asynchronously under program control, or synchronously as part of a digital scan group.

The **CTR0** and **CTR1** terminals are 32-bit general-purpose counters that can accept frequency inputs up to 50 MHz.

The USB-1808 supports the following counter input modes:

- Totalize
- Period measurement
- Pulse-width measurement

Counter input modes are programmable with software. Each mode supports additional counter operation options.

Typically, when data is acquired with no counter operation options set, the count of each counter channel is set to 0 and latched at the beginning of the acquisition.

When counter options are set the counters can concurrently monitor time periods, frequencies, pulses, and other event-driven incremental occurrences directly from pulse-generators, limit switches, proximity switches, and magnetic pick-ups.

Counter input operations can be paced by the internal clock or by an external clock (**ICLKI** – refer to *Clock I/O* on page 15). They can be initiated by a digital trigger (*Digital triggering* on page 15) or a pattern trigger (*Pattern triggering* on page 15).

Refer to *Synchronous I/O – mixing analog, digital, and counter scanning* on page 15 for information on running counter input scans at the same time as other subsystem scans.

Totalize counter mode

The USB-1808 can be used as a high-speed pulse counter for general counting applications. The internal counter increments when the TTL levels transition from low to high or from high to low.

Each option supported in Totalize mode is explained in following table:

Totalize counter mode options

Counter option	Description
Clear on read	The counter is cleared after each read (synchronous or asynchronous). The value of the counter before it was cleared is latched and returned.
Range limit	When counting up: The counter rolls over to MINLIMIT (or stops if Non-recycle is set) when the maximum count (specified by the MAXLIMIT value) is reached. When counting down: The counter counts down to MINLIMIT and then rolls over to MAXLIMIT (or stops if Non-recycle is set).
Non-recycle	The counter stops if a count overflow or underflow occurs (or, if Range limit is set, the MAXLIMIT or MINLIMIT value is reached). Counting resumes if direction is reversed or the counter is reloaded.

Period measurement mode

Use period mode to measure the period of a signal at a counter channel's input. You can measure x1, x10, x100 or x1000 periods for 32-bit values. Four resolutions are available — 20 ns, 200 ns, 2000 ns, or 20,000 ns. All period measurement mode options are software-selectable. The 100 MHz system clock is used as the timing source. Periods from sub-microsecond to many seconds can be measured.

Pulse width measurement mode

Use pulse width mode to measure the time from the rising edge to the falling edge, or vice versa, on a signal on a counter input. Four resolutions are available — 20 ns, 200 ns, 2000 ns, or 20,000 ns. All pulse width measurement mode options are software selectable. The 100 MHz system clock is used as the timing source. Pulse widths from sub-microsecond to many seconds can be measured.

Quadrature encoder input

The USB-1808 can simultaneously decode signals from up to two encoders. Quadrature encoders, 50 MHz maximum pulse frequency, and X1, X2, and X4 count modes are supported.

The USB-1808 provides A, B, and Z inputs – ENCxA, ENCxB, and ENCxZ – for each connected encoder. A typical encoder generates the A and B signals at a 90° phase shift with respect to each other. These signals are used to determine system position (counts), velocity (counts per second), and direction of travel or rotation. The Z signal can be programmed to latch the current count or reload the counter with the MINLIMIT value (counting up) or the MAXLIMIT value (counting down).

The Z signal may be used to establish an absolute reference position within one count of the encoder travel or rotation. This signal can be used to reload the position counter, which is useful at system startup when the incremental encoder cannot determine the starting position.

Encoder input operations can be paced by the internal clock or by an external clock (**ICLKI** – refer to *Clock I/O* on page 15). They can be initiated by a digital trigger (*Digital triggering* on page 15) or a pattern trigger (*Pattern triggering* on page 15).

Refer to *Synchronous I/O – mixing analog, digital, and counter scanning* on page 15 for information on running quadrature encoder scans at the same time as other subsystem scans.

Each supported quadrature encoder option is explained in following table:

Quadrature encoder options

Encoder option	Description
Count mode	Select X1, X2, or X4. Count modes provide different levels of accuracy with respect to the encoder position. ■ X1: counts rising edges on input A. ■ X2: counts rising edges and falling edges on input A. ■ X4: count rising and falling edges on both inputs A and B.
Range limit	When counting up: The counter stops when the maximum count (specified by the MAXLIMIT value) is reached. Counting resumes if direction is reversed or the counter is cleared. When counting down: The counter stops when the minimum count (specified by the MINLIMIT value) is reached. Counting resumes if direction is reversed or the counter is cleared.

Quadrature encoder options that are specific to the Z signal (ENCxZ) are is explained in following table.

Z input quadrature encoder options ()

Counter mode	Description
Clear on Z	The counter is cleared by the Z signal.
Latching	Latching mode allows the count to be latched by the Z signal.

Timer output

You can use **TMR0** through **TMR1** as 32-bit timer outputs. Each timer can generate pulse rates of up to 50 MHz, with programmable pulse widths down to 10 ns.

The timer output rate and pulse width can be updated asynchronously at any time, however, doing so results in a pulse stream that is not seamless.

The following timer output options are software-selectable:

- pulse frequency
- duty cycle (pulse width divided by the pulse period)
- number of pulses to generate
- time delay before starting the timer output after it is enabled
- idle state of the output (idle high or idle low)

The time delay can range from 0 seconds to 42.94 seconds.
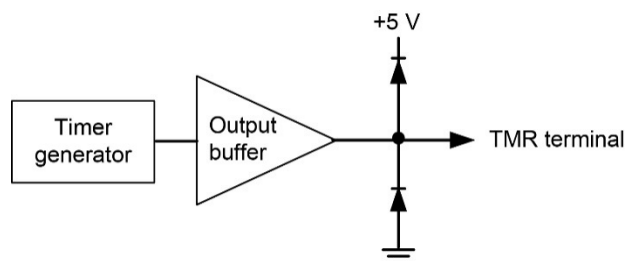

Figure 8. USB-1808 PWM timer channel

Timer output operations can be paced by the internal clock or by an external clock (**OCLKI** – refer to *Clock I/O* on page 15). They can be initiated by a digital trigger (*Digital triggering* on page 15).

Synchronous I/O – mixing analog, digital, and counter scanning

The USB-1808 can read analog, digital, and counter inputs, and generate up to two analog outputs and one digital pattern output at the same time. Digital and counter inputs do not affect the overall A/D rate because these inputs use no time slot in the scanning sequencer.

For example, one analog input channel can be scanned at the full 50 kS/s A/D rate along with digital and counter input channels. Each analog channel can have a different gain, and counter and digital channels do not need additional scanning bandwidth if there is at least one analog channel in the scan group. Digital input channel sampling is done during the *dead time* of the scan period when no analog sampling is being done.

Clock I/O

The USB-1808 provides one external clock input (**ICLKI**) and one clock output (**ICLKO**) for input operations.

- Connect an external clock signal to **ICLKI**.
- The pacer clock is available at **ICLKO**.

The USB-1808 provides one external clock input (**OCLKI**) and one clock output (**OCLKO**) for output operations.

- Connect an external clock signal to **OCLKI**.
- The pacer clock is available at **OCLKO**.

Digital triggering

The **ITRIG** (for triggering input operations) and **OTRIG** (for triggering output operations) terminals are external digital trigger inputs. The trigger mode is software-selectable for edge or level sensitive. Edge sensitive mode is selectable for rising or falling. Level sensitive mode is selectable for high or low.

Pattern triggering

You can also start an input or output scan with a digital pattern trigger using DIO0 – DIO3. The pattern represents the state of up to four bits on the port.

You specify the pattern and the trigger type with software. Supported trigger types are Above Pattern, Below Pattern, Equal Pattern, and Not Equal Pattern. The scan begins when the trigger conditions are met.

The base clock is fixed at 100 MHz (10 ns). The trigger pattern must be held for five base clock cycles (50 ns) to ensure that it is properly detected. The trigger latency is 1 scan clock period + 8 base clock cycles (80 ns).

Mask option

Use a bitmask to specify which bits to include or exclude from the pattern to detect. To include a bit in the pattern, sets its value to 1. To exclude a bit from the pattern, sets its value to 0. Refer to the pattern and mask values shown in Figure 9 and Figure 10.

In Figure 9 all mask bits are set to 1, so all the bits are included in the pattern to detect.

<div align="center">

Bit   Bit
3   0

Pattern 1010

Mask <u>1111</u> (AND)

1010

</div>

Figure 9. Trigger mask with all bits included

In Figure 10 all mask bits are excluded except bit 3. The result of this operation is that only bit 3 is included in the pattern to detect.

$$
\begin{array}{c}
\overset{\text{Bit}}{3} \qquad \overset{\text{Bit}}{0} \\
\text{Pattern}\quad 1010 \\
\text{Mask}\quad \underline{1000}\ \text{(AND)} \\
1000
\end{array}
$$

Figure 10. Trigger mask with some bits excluded

Ground

The analog ground (**AGND**) terminals provide a common ground for all analog channels.

The digital ground (**GND**) terminals provide a common ground for the digital, trigger, counter, and encoder terminals.

Power output

The **+VO** terminal can output up to 10 mA maximum. You can use this terminal to supply power to external devices or circuitry.
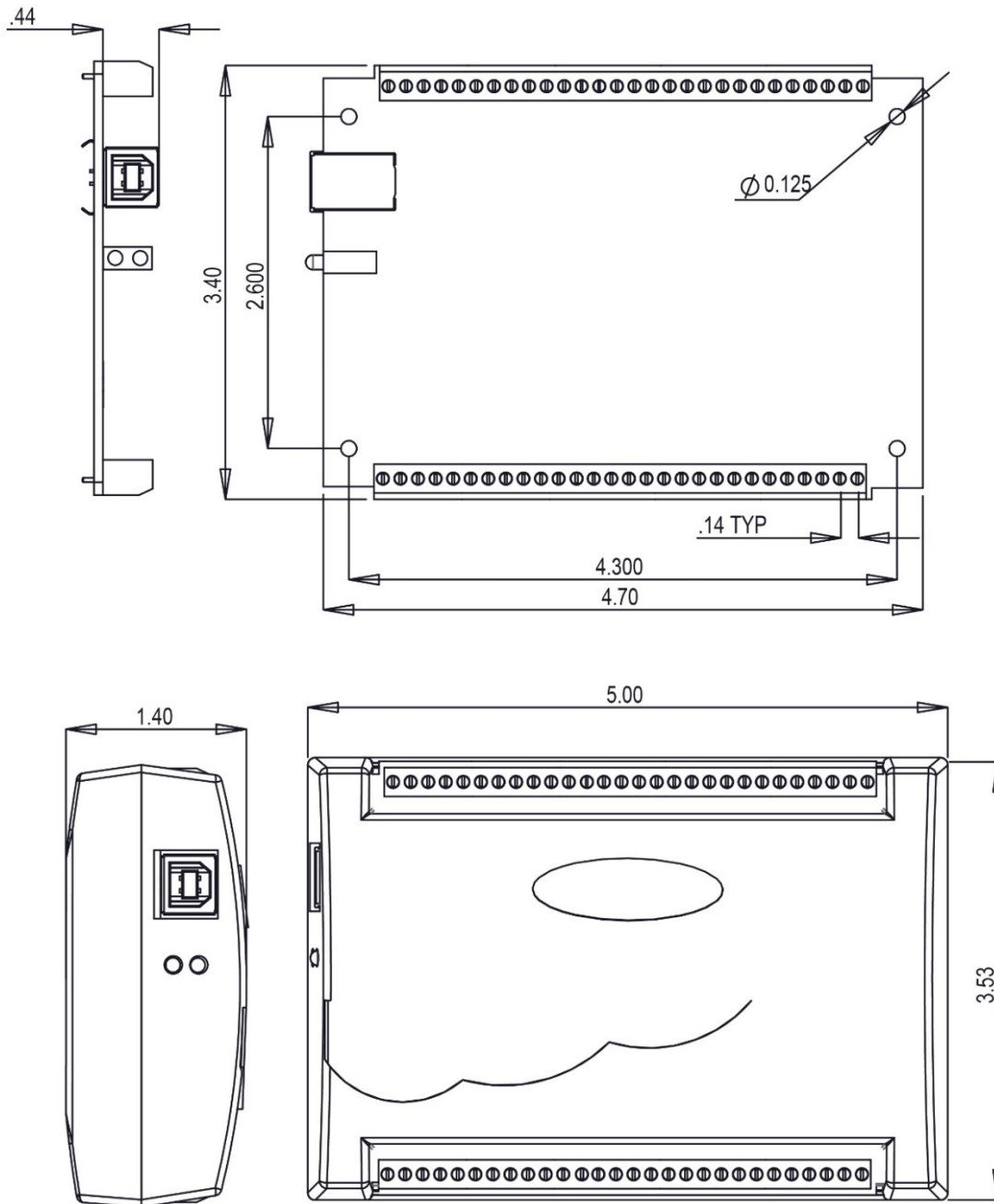
Mechanical drawings

Figure 11. USB-1808 circuit board (top) and enclosure dimensions

Specifications

All specifications are subject to change without notice.
Typical for 25 °C unless otherwise specified.
Specifications in *italic* text are guaranteed by design.

Analog input

Table 1. General analog input specifications

Parameter	Condition	Specification
A/D converter type		Simultaneous
ADC resolution		18 bits
Number of channels		8 differential (DIFF), 8 single-ended (SE); software-selectable per-channel for SE or DIFF
Input voltage range		±10 V, ±5 V, 0 V to 10 V, 0 V to 5 V Software-selectable per channel
Absolute max input voltage	*CHx relative to AGND*	■ *±25 V max (power on)* ■ *±15 V max (power off)*
Input impedance		■ *>1 GΩ (power on)* ■ *1000 Ω (power off)*
Input bias current		*±50 pA*
Input bandwidth	All input ranges, small signal (−3 dB)	2.0 MHz
Input capacitance		*50 pf*
Common mode voltage range	±10 V range	±10.1 V
	±5 V range	±10.1 V
	0 V to 10 V range	±10.1 V
	0 V to 5 V range	±10.1 V
Common mode rejection ratio	$f_{IN} \leq 1$ kHz, all input ranges	90 dB
Crosstalk	±10 V, adjacent channels, DC to 100 kHz	−95 dB
Input coupling		DC
Sample rate		0.023 Hz to 50 kHz; software-selectable
Scan clock source		Internal input scan clock or external input scan clock (ICLKI pin)
Trigger source		■ ITRIG (see *External trigger* on page 24) ■ Digital pattern detection (see *Pattern trigger* on page 24)
Channel gain queue	Up to 8 elements	Software-selectable. Queue list may contain up to eight elements of unique, consecutive channels paired with any valid range.
Warm-up time		15 minutes min

Accuracy

Analog input DC voltage measurement accuracy

Table 2. DC accuracy components and specifications. All values are (±)

Range	Gain error (% of reading)	Offset error (mV)	INL error (% of range)	Absolute accuracy at Full Scale (mV)	Gain temperature coefficient (% reading/°C)	Offset temperature coefficient (µV/°C)
±10 V	0.020	1.5	0.00076	3.576	0.00023	4
±5 V	0.020	1.0	0.00057	2.028	0.00023	4
0 V to 10 V	0.020	1.5	0.00028	3.528	0.00023	4
0 V to 5 V	0.020	1.0	0.00014	2.007	0.00023	4

Dynamic performance

Table 3. Dynamic performance specifications

Range	Condition	Specification
±10 V	Signal-to-noise ratio (SNR)	94 dB
	Signal-to-noise-and-distortion ratio (SINAD)	94 dB
	Total harmonic distortion (THD)	–108 dB
	Spurious free dynamic range (SFDR)	112 dB
	Effective number of bits (ENOB)	15.3 bits
±5 V	SNR	91 dB
	SINAD	91 dB
	THD	–105 dB
	SFDR	107 dB
	ENOB	14.8 bits
0 V to 10 V	SNR	87 dB
	SINAD	87 dB
	THD	–104 dB
	SFDR	109 dB
	ENOB	14.5 bits
0 V to 5 V	SNR	83 dB
	SINAD	83 dB
	THD	–103 dB
	SFDR	103 dB
	ENOB	13.6 bits

Noise performance

For the peak-to-peak noise distribution test, a differential input channel is connected to AGND at the input terminal block, and 32,000 samples are acquired at the maximum rate available at each setting.

Table 4. Noise performance specifications

Range	Counts	LSBrms
±10 V	11.6	1.77
±5 V	18.0	2.73
0 V to 10 V	23.3	3.54
0 V to 5 V	36.1	5.47

Analog output

Table 5. Analog output specifications

Parameter	Condition	Specification
Number of channels		2
Resolution		16 bits
Output ranges	Calibrated	±10 V
Output transient	Host computer is reset, powered on, suspended, or a reset command is issued to the device	Duration: 5 ms Amplitude: 2 V p-p
	Powered off from 0 V output	Duration: 20 ms Amplitude: 5 V p-p
Differential non-linearity		±0.25 LSB typ ±1 LSB max
Output current	AOUTx pins	±3.5 mA max
Output short-circuit protection	Single AOUTx channel connected to AGND	Unlimited duration
Output coupling		DC
Power on and reset state		DACs cleared to zero-scale: 0 V, ±50 mV
Output noise		100 µVrms
Trigger source		■ OTRIG (see *External trigger* on page 24) ■ Digital pattern detection (see *Pattern trigger* on page 24)
Scan clock source		Internal output scan clock or external output scan clock (OCLKI pin)
Output update rate		0.023 Hz to 125 kHz per channel
Slew rate		*15 V/µS*
Throughput	Software paced	33 S/s to 8,000 S/s typ, system-dependent
	Hardware paced	250 kS/s max, system-dependent

Note 1: Leave unused AOUTx output channels disconnected.

Note 2: AOUTx defaults to 0 V whenever the host computer is reset, powered on, suspended, or a reset command is issued to the device.

Table 6. Calibrated absolute accuracy specifications

Range	Absolute accuracy (±LSB)
±10 V	16

Table 7. Calibrated absolute accuracy components specifications

Range	% of reading	Offset (±mV)	Offset tempco (µV/°C)	Gain tempco (ppm of range/°C)
±10 V	0.0183	1.831	4.7	9.4

Table 8. Relative accuracy specifications (±LSB)

Range	Relative accuracy (INL)
±10 V	1.0

Analog input/output calibration

Table 9. Analog I/O calibration specifications

Parameter	Specification
Warm-up time	15 minutes recommended min
Calibration method	Factory calibration
Calibration interval	1 year

Digital input/output

Table 10. Digital I/O specifications

Parameter	Specification
Digital type	CMOS
Number of I/O	4
Configuration	Each bit may be configured as input (power on default) or output
Pull-up configuration	The port has 47 kΩ resistors configurable as pull-up or pull-down (default) via internal jumper (DIO).
Digital I/O transfer rate (system-paced, asynchronous)	33 to 8,000 port reads/writes or single bit reads/writes per second typ, system dependent.
Digital I/O transfer rate (synchronous)	0.023 Hz to 50 kHz input, 125 kHz output, based on the internal clock speed of 100 MHz
Scan clock source for input	Internal input scan clock or external input scan clock (ICLKI pin)
Scan clock source for input	Internal output scan clock or external output scan clock (OCLKI pin)
Trigger source	■ ITRIG for inputs, OTRIG for outputs (see *External trigger* on page 24) ■ Digital pattern detection for inputs and outputs (see *Pattern trigger* on page 24)
Input high voltage	2.0 V min 5.5 V absolute max
Input low voltage	0.8 V max –0.5 V absolute min 0 V recommended min
Output high voltage	4.4 V min (IOH = –50 µA) 3.76 V min (IOH = –2.5 mA)
Output low voltage	0.1 V max (IOL = 50 µA) 0.44 V max (IOL = 2.5 mA)
Output current	±2.5 mA max

Counter

Table 11. Counter specifications

Parameter	Specification
Terminal names	CTR0, CTR1
Number of channels	2 channels
Resolution	32-bit
Counter type	FPGA
Counter input modes	Totalize, Pulse width, Period
Input type	Schmitt trigger, 33 Ω series resistor, 47 kΩ pull-down to ground
Input source	CTR0 CTR1
Scan clock source	Internal input scan clock or external input scan clock (ICLKI pin)
Trigger source	■ ITRIG (see *External trigger* on page 24) ■ Digital pattern detection (see *Pattern trigger* on page 24)
Counter read clock	Internal or external input scan clock up to 50 kHz
Period/pulse width resolution	20 ns, 200 ns, 2 µs or 20 µs; software-selectable
Input high voltage	2.2 V min, 5.5 V max
Input low voltage	1.5 V max, –0.5 V min
Schmitt trigger hysteresis	0.4 V min, 1.2 V max
Input frequency	50 MHz, max
Schmitt trigger hysteresis	0.76 V typ 0.4 V min 1.2 V max
Input high voltage threshold	1.74 V typ 1.3 V min 2.2 V max
Input low voltage threshold	0.98 V typ 0.6 V min 1.5 V max
Input low voltage limit	–0.5 V absolute min 0 V recommended min

Quadrature inputs

Table 12. Quadrature input specifications

Parameter	Specification
Terminal names	ENC0A, ENC0B, ENC0Z; ENC1A, ENC1B, ENC1Z
Number of encoders	2
Signals per encoder	A, B and Z
Resolution	20 ns
Maximum frequency	50 MHz
Minimum pulse width	*10 ns*
De-bounce function	None
Scan clock source	Internal input scan clock or external input scan clock (ICLKI pin)
Trigger source	■ ITRIG (see *External trigger* on page 24) ■ Digital pattern detection (see *Pattern trigger* on page 24)
Input high voltage	2.2 V min, 5.5 V max
Input low voltage	1.5 V max, –0.5 V min
Absolute maximum input voltage	5.5 V

Timer

Table 13. Timer specifications

Parameter	Specification
Terminal name	TMR0, TMR1
Timer type	PWM output with count, period, delay, and pulse width registers
Output value	Default state is idle low with pulses high, software-selectable output invert
Trigger source	OTRIG (see *External trigger* on page 24)
Internal clock frequency	100 MHz
Register widths	32-bit
High pulse width	*10 ns min*
Low pulse width	*10 ns min*
Output high voltage	4.4 V min (IOH = –50 µA) 3.76 V min (IOH = –2.5 mA)
Output low voltage	0.1 V max (IOL = 50 µA) 0.44 V max (IOL = 2.5 mA)
Output current	±2.5 mA max

External clock input/output

Table 14. External clock I/O specifications

Parameter	Specification	
Terminal names	ICLKI, ICLKO OCLKI, OCLKO	
Terminal types	xCLKI: xCLKO:	Input, active on rising edge Output, power on default is 0 V, active on rising edge
Terminal descriptions	xCLKI:	Receives sampling clock from external source
	xCLKO:	Outputs the internal input scan or internal output scan clock, or the pulse generated from xCLKI when in external clock mode.
Input clock rate	125 kHz max	
Clock pulse width	xCLKI:	400 ns min
	xCLKO:	400 ns min
Input type	Schmitt trigger, 33 Ω series resistor, 47 kΩ pull-down to ground	
Schmitt trigger hysteresis	0.4 V to 1.2 V	
Input high voltage	2.2 V min 5.5 V absolute max	
Input low voltage	1.5 V max –0.5 V absolute min 0 V recommended min	
Output high voltage	4.4 V min (IOH = –50 µA) 3.76 V min (IOH = –2.5 mA)	
Output low voltage	0.1 V max (IOL = 50 µA) 0.44 V max (IOL = 2.5 mA)	
Output current	±2.5 mA max	

External trigger

Table 15. External trigger specifications

Parameter	Specification
Trigger source	ITRIG for inputs, OTRIG for outputs
Trigger mode	Software programmable for edge or level sensitive, rising or falling edge, high or low level. Power on default is edge sensitive, rising edge.
Trigger latency	1 µs + 1 clock cycle max
Trigger pulse width	100 ns min
Input type	Schmitt trigger, 33 Ω series resistor and 49.9 kΩ pull-down to ground
Schmitt trigger hysteresis	0.4 V to 1.2 V
Input high voltage	2.2 V min 5.5 V absolute max
Input low voltage	1.5 V max –0.5 V absolute min 0 V recommended min

Pattern trigger

Table 16. Pattern trigger specifications

Parameter	Specification
Trigger source	DIO0 – DIO3
Trigger types	Above pattern, Below pattern, Equal pattern, or Not equal pattern
Trigger stability	Digital port must be stable for 50 ns to be recognized as a pattern
Trigger bit width	Up to 4, adjustable through bitmask
Trigger latency	Up to 1 scan period

Memory

Table 17. Memory specifications

Parameter	Specification
Data FIFO	4 kS analog input/2 kS analog output
Non-volatile memory	32 KB (28 KB firmware storage, 4 KB calibration/user data)

Power

Table 18. Power specifications

Parameter	Condition	Specification
Supply current (Note 3)	Quiescent current	305 mA
+VO user output voltage range (Note 4)	Available at connector pin 13	4.5 V min to 5.25 V max
+VO user output current	Available at connector pin 13	10 mA max

Note 3: This is the total quiescent current requirement for the device that includes up to 10 mA for the status LED. This does not include any potential loading of the digital I/O bits, +VO terminal, or the AOUTx outputs.

Note 4: The +4.5 V min limit includes the +VO 10 mA load, it does not include any potential loading of the digital I/O bits or the AOUTx outputs.

USB

Table 19. USB specifications

Parameter	Specification
USB device type	USB 2.0 (high-speed)
Device compatibility	USB 1.1, USB 2.0, USB 3.0
USB cable type	A-B cable, UL type AWM 2725 or equivalent. (Min 24 AWG VBUS/GND, min 28 AWG D+/D–)
USB cable length	3 m (9.84 ft) max

Environmental

Table 20. Environmental specifications

Parameter	Specification
Operating temperature range	0 °C to 55 °C max
Storage temperature range	–40 °C to 85 °C max
Humidity	0% to 90% non-condensing max

Mechanical

Table 21. Mechanical specifications

Parameter	Specification
Dimensions (L × W × H)	127 × 89.9 × 35.6 mm (5.00 × 3.53 × 1.40 in.)
User connection length	3 m (9.84 ft) max

Screw terminal connector

Table 22. Screw terminal connector specifications

Parameter	Specification
Connector type	Screw terminal
Wire gauge range	16 AWG to 30 AWG

Differential mode pinout

Table 23. 8-channel differential mode pinout

#	Label	Use	#	Label	Use
1	CH0H	AI channel 0 HI	29	CH7L	AI channel 7 LO
2	CH0L	AI channel 0 LO	30	CH7H	AI channel 7 HI
3	AGND	Analog ground	31	AGND	Analog ground
4	CH1H	AI channel 1 HI	32	CH6L	AI channel 6 LO
5	CH1L	AI channel 1 LO	33	CH6H	AI channel 6 HI
6	AGND	Analog ground	34	AGND	Analog ground
7	CH2H	AI channel 2 HI	35	CH5L	AI channel 5 LO
8	CH2L	AI channel 2 LO	36	CH5H	AI channel 5 HI
9	AGND	Analog ground	37	AGND	Analog ground
10	CH3H	AI channel 3 HI	38	CH4L	AI channel 4 LO
11	CH3L	AI channel 3 LO	39	CH4H	AI channel 4 HI
12	AGND	Analog ground	40	AGND	Analog ground
13	+VO	+5V power output	41	AOUT0	AO channel 0
14	AGND	Analog ground	42	AOUT1	AO channel 1
15	GND	Digital Ground	43	AGND	Analog ground
16	TMR0	Timer 0 output	44	GND	Digital Ground
17	TMR1	Timer 1 output	45	DIO0	DIO channel 0
18	ICLKO	Input scan clock output	46	DIO1	DIO channel 1
19	OCLKO	Output scan clock output	47	GND	Digital Ground
20	GND	Digital ground	48	DIO2	DIO channel 2
21	ICLKI	Input scan clock input	49	DIO3	DIO channel 3
22	OCLKI	Output scan clock input	50	GND	Digital Ground
23	ITRIG	Input Trigger	51	CTR0	Counter 0 input
24	OTRIG	Output Trigger	52	CTR1	Counter 1 input
25	GND	Digital ground	53	GND	Digital ground
26	ENC1A	Encoder 1 Input A	54	ENC0A	Encoder 0 Input A
27	ENC1B	Encoder 1 Input B	55	ENC0B	Encoder 0 Input B
28	ENC1Z	Encoder 1 Input Z	56	ENC0Z	Encoder 0 Input Z

Single-ended mode pinout

Table 24. 16-channel single-ended mode pinout

Terminal			Terminal		
#	Label	Use	#	Label	Use
1	CH0H	AI channel 0 HI	29	NC	No connection
2	NC	No connection	30	CH7H	AI channel 7 HI
3	AGND	Analog ground	31	AGND	Analog ground
4	CH1H	AI channel 1 HI	32	NC	No connection
5	NC	No connection	33	CH6H	AI channel 6 HI
6	AGND	Analog ground	34	AGND	Analog ground
7	CH2H	AI channel 2 HI	35	NC	No connection
8	NC	No connection	36	CH5H	AI channel 5 HI
9	AGND	Analog ground	37	AGND	Analog ground
10	CH3H	AI channel 3 HI	38	NC	No connection
11	NC	No connection	39	CH4H	AI channel 4 HI
12	AGND	Analog ground	40	AGND	Analog ground
13	+VO	+5V power output	41	AOUT0	AO channel 0
14	AGND	Analog ground	42	AOUT1	AO channel 1
15	GND	Digital Ground	43	AGND	Analog ground
16	TMR0	Timer 0 output	44	GND	Digital Ground
17	TMR1	Timer 1 output	45	DIO0	DIO channel 0
18	ICLKO	Input scan clock output	46	DIO1	DIO channel 1
19	OCLKO	Output scan clock output	47	GND	Digital Ground
20	GND	Digital ground	48	DIO2	DIO channel 2
21	ICLKI	Input scan clock input	49	DIO3	DIO channel 3
22	OCLKI	Output scan clock input	50	GND	Digital Ground
23	ITRIG	Input Trigger	51	CTR0	Counter 0 input
24	OTRIG	Output Trigger	52	CTR1	Counter 1 input
25	GND	Digital ground	53	GND	Digital ground
26	ENC1A	Encoder 1 Input A	54	ENC0A	Encoder 0 Input A
27	ENC1B	Encoder 1 Input B	55	ENC0B	Encoder 0 Input B
28	ENC1Z	Encoder 1 Input Z	56	ENC0Z	Encoder 0 Input Z

CE EU Declaration of Conformity
According to ISO/IEC 17050-1:2010

Manufacturer:	Measurement Computing Corporation
Address:	10 Commerce Way
	Norton, MA 02766
	USA
Product Category:	Electrical equipment for measurement, control and laboratory use.
Date and Place of Issue:	March 23, 2017, Norton, Massachusetts USA
Test Report Number:	EMI6990.17

Measurement Computing Corporation declares under sole responsibility that the product

USB-1808

is in conformity with the relevant Union Harmonization Legislation and complies with the essential requirements of the following applicable European Directives:

Electromagnetic Compatibility (EMC) Directive 2014/30/EU

Low Voltage Directive 2014/35/EU

RoHS Directive 2011/65/EU

Conformity is assessed in accordance to the following standards:

EMC:

Emissions:

- EN 61326-1:2013 (IEC 61326-1:2012), Class A
- EN 55011: 2009 + A1:2010 (IEC CISPR 11:2009 + A1:2010), Group 1, Class A

Immunity:

- EN 61326-1:2013 (IEC 61326-1:2012), Controlled EM Environments
- EN 61000-4-2:2008 (IEC 61000-4-2:2008)
- EN 61000-4-3 :2010 (IEC61000-4-3:2010)

Safety:

- EN 61010-1 (IEC 61010-1)

Environmental Affairs:

Articles manufactured on or after the Date of Issue of this Declaration of Conformity do not contain any of the restricted substances in concentrations/applications not permitted by the RoHS Directive.

Carl Haapaoja, Director of Quality Assurance