Register Map for the PCI-DIO96

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Register Description

The PCI-DIO96 design implements a PLX Technology PCI-9052 PCI controller and uses three base address regions (Table 1). They are described in the following section. An explanation of the operation of the PCI-9052 is beyond the scope of this document. For more information about the PCI-9052 and its programming, refer to the manufacturer's data sheet at www.plxtech.com/products/io_accelerators/PCI9052/default.htm.

Table 1. I/O Region register operations

I/O Region	Function	Operations
BADR0	PCI memory-mapped configuration registers	32-bit double word
BADR1	PCI I/O-mapped configuration registers	32-bit double word
BADR2	N/A	N/A
BADR3	Digital I/O registers	8-bit byte

BADR0

BADR0 registers are for memory access to the local configuration registers. There is no reason to access this region of I/O space. The PCI-DIO96 design implements I/O access only.

BADR1

BADR1 registers are for I/O access to the local configuration registers.

INTCSR (Interrupt Control/Status Register)

BADR1 +4C hex

32:15	14	13	12	11	10	9	8
X	X	X	ISAMD	X	INTCLR	X	LEVEL/EDGE

Read/Write

7	6	5	4	3	2	1	0
X	PCINT	X	X	X	INT	INTPOL	INTE

Note: For applications requiring edge triggered interrupts (LEVEL/EDGE bit 8 = 1), the user must configure the INTPOL bit for active high polarity (bit 1=1).

The INTCSR (Interrupt Control/Status Register) controls the interrupt features of the PLX PCI 9052 controller. As with all of the PLX PCI-9052 registers, it is 32-bits in length. Since the rest of the bits in the register have specific control functions, those bits must be masked off in order to access the specific interrupt control functions listed below.

INTE — Interrupt enable (local):

0 = disabled

1 = enabled (default)

INTPOL — Interrupt polarity:

0 = active low (default)

1 = active high

INT — Interrupt status:

0 = interrupt not active

1 = interrupt active

PCINT	PCI interrupt enable:
	0 = disabled (default)
	1 = enabled
LEVEL/EDGE	Interrupt trigger control:
	0 = level triggered mode (default)
	1 = edge triggered mode
INTCLR	Interrupt clear (edge triggered mode only):
	0 = N/A, 1 = clear interrupt
ISAMD	ISA mode enable control (must be set to 1)
	0 = ISA mode disabled, 1 = ISA mode enabled (default)

BADR2

BADR2 is not used.

BADR3

BADR3 is an 8-bit address space for reading, writing and control of the individual 82C55 and 82C54 chips. Refer to Table 2 for specific register offsets.

Table 2. BADR3 Registers

Register	Read Function	Write Function
BADR3 + 0	Group 0 Port A Data	Group 0 Port A Data
BADR3 + 1	Group 0 Port B Data	Group 0 Port B Data
BADR3 + 2	Group 0 Port C Data	Group 0 Port Data
BADR3 + 3	Group 0 Configure	Group 0 Configure
BADR3 + 4	Group 1 Port A Data	Group 1 Port A Data
BADR3 + 5	Group 1 Port B Data	Group 1 Port B Data
BADR3 + 6	Group 1 Port C Data	Group 1 Port C Data
BADR3 + 7	Group 1 Configure	Group 1 Configure
BADR3 + 8	Group 2 Port A Data	Group 2 Port A Data
BADR3 + 9	Group 2 Port B Data	Group 2 Port B Data
BADR3 + A	Group 2 Port C Data	Group 2 Port C Data
BADR3 + B	Group 2 Configure	Group 2 Configure
BADR3 + C	Group 3 Port A Data	Group 3 Port A Data
BADR3 + D	Group 3 Port B Data	Group 3 Port B Data
BADR3 + E	Group 3 Port C Data	Group 3 Port C Data
BADR3 + F	Group 3 Configure	Group 3 Configure
BADR3 + 10h	Counter 1	Counter 1
BADR3 + 11h	Counter 2	Counter 2
BADR3 + 12h	N/A	N/A
BADR3 + 13h	Counter Configuration	Counter Configure
BADR3 + 14h	Interrupt Control 1	Interrupt Control 1
BADR3 + 15h	Interrupt Control 2	Interrupt Control 2

The 82C55 may be programmed to operate in Input/Output (mode 0), Strobed Input/Output (mode 1) or Bi-Directional Bus (mode 2). The following information describes mode 0 operation. Users needing information regarding other modes of operation should refer to an Intel or Intersil 82C55 data sheet.

For more information on I/O configuration of the 82C55 refer to the PDF document *82C55A CMOS Programmable Interface* at www.measurementcomputing.com/82C55.

Upon power-up, an 82C55 is reset and defaults to the input mode. No further programming is needed to use the 24 lines of an 82C55 as TTL inputs.

Group 0 8255 Configuration and Data

Group 0, Port A Data

BADR3 + 0

Read/Write

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Group 0, Port B Data

BADR3 + 1

Read/Write

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Group 0, Port C Data

BADR3 + 2

Read/Write

7	6	5	4	3	2	1	0
C8	C7	C6	C5	C4	C3	C2	C1
CH4	CH3	CH2	CH1	CL4	CL3	CL2	CL1

Group 0 Configure

BADR3 + 3

Read/Write

7	6	5	4	3	2	1	0
MS	M3	M2	A	CH	M1	B	CL

This register is used to configure the Group 0 ports as either input or output, and configures the operating mode to mode 0, 1 or 2. The following describes configuration for mode 0. See the Intel or Harris 8255 data sheets for information on other modes of operation

8255 Mode 0 configuration

Output Ports

In mode 0 configuration, 82C55 ports can be configured as outputs, holding the data written to them. For example, to set all three ports (A, B, & C) of Group 0 to output mode, write the value 80 hex to BADR3 + 3 (refer to Table 5-3 below). The user is then able to read the current state of each output port by simply reading the address corresponding to that port.

Input Ports

In mode 0 configuration, the 82C55 ports can be configured as inputs, reading the state of the input lines. For example, to set all of the ports of Group 0 to the input mode, write the value 9B hex to BADR3 + 3.

Table 3. DIO Port Configurations/Per Group

Programming Codes						Values			
D4	D3	D1	D0	Hex	Dec	A	B	CU	CL
0	0	0	0	80	128	OUT	OUT	OUT	OUT
0	0	0	1	81	129	OUT	OUT	OUT	IN
0	0	1	0	82	130	OUT	IN	OUT	OUT
0	0	1	1	83	131	OUT	IN	OUT	IN
0	1	0	0	88	136	OUT	OUT	IN	OUT
0	1	0	1	89	137	OUT	OUT	IN	IN
0	1	1	0	8A	138	OUT	IN	IN	OUT
0	1	1	1	8B	139	OUT	IN	IN	IN
1	0	0	0	90	144	IN	OUT	OUT	OUT
1	0	0	1	91	145	IN	OUT	OUT	IN
1	0	1	0	92	146	IN	IN	OUT	OUT
1	0	1	1	93	147	IN	IN	OUT	IN
1	1	0	0	98	152	IN	OUT	IN	OUT
1	1	0	1	99	153	IN	OUT	IN	IN
1	1	1	0	9A	154	IN	IN	IN	OUT
1	1	1	1	9B	155	IN	IN	IN	IN

Notes: "CU" is PORT C upper nibble, and "CL" is PORT C lower nibble.

Group 1 8255 Configuration and Data

Group 1, Port A Data

BADR3 + 4

Read/Write

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Group 1, Port B Data

BADR3 + 5

Read/Write

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Group 1, Port C Data

BADR3 + 6

Read/Write

7	6	5	4	3	2	1	0
C8	C7	C6	C5	C4	C3	C2	C1
CH4	CH3	CH2	CH1	CL4	CL3	CL2	CL1

Group 1 Configure

BADR3 + 7

Read/Write

7	6	5	4	3	2	1	0
MS	M3	M2	A	CH	M1	B	CL

Group 2 8255 Configuration and Data

Group 2, Port A Data

BADR3 + 8

Read/Write

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Group 2, Port B Data

BADR3 + 9

Read/Write

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Group 2, Port C Data

BADR3 + A hex

Read/Write

7	6	5	4	3	2	1	0
C8	C7	C6	C5	C4	C3	C2	C1
CH4	CH3	CH2	CH1	CL4	CL3	CL2	CL1

Group 2 Configure

BADR3 + B hex

Read/Write

7	6	5	4	3	2	1	0
MS	M3	M2	A	CH	M1	B	CL

Group 3 8255 Configuration and Data

Group 3, Port A Data

BADR3 + C hex

Read/Write

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Group 3, Port B Data

BADR3 + D hex

Read/Write

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Group 3, Port C Data

BADR3 + E hex

Read/Write

7	6	5	4	3	2	1	0
C8	C7	C6	C5	C4	C3	C2	C1
CH4	CH3	CH2	CH1	CL4	CL3	CL2	CL1

Group 3 Configure

BADR3 + F hex

Read/Write

7	6	5	4	3	2	1	0
MS	M3	M2	A	CH	M1	B	CL

8254 Configuration and Data

Counter 1 Data

BADR3 + 10 hex

Read/Write

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

The 82C54 counters 1 and 2 have been configured in hardware to produce a 32-bit counter for use in interrupt generation. This register provides access to the *lower* 16 data bits. Since the interface to the 82C54 is only 8-bits wide, write counter data in two bytes; low byte first, followed by the high byte.

Counter 2 Data

BADR3 + 11 hex

Read/Write

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

The 82C54 counters 1 and 2 have been configured in hardware to produce a 32-bit counter for use in interrupt generation. This register provides access to the *upper* 16 data bits. Since the interface to the 82C54 is only 8-bits wide, write counter data in two bytes; low byte first, followed by the high byte.

Counter Configuration

BADR3 + 13 hex

Read/Write

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

This register is used to set the operating modes of each of the 82C54's counters. Configure the counters by writing mode information to the counter configuration register, followed by the count information written to the specific counter (data) registers. Refer to the Celeritous 82C54 data sheet at www.celeritous.com for more detailed information.

Interrupt Control 1

BADR3 + 14 hex

Read/Write

7	6	5	4	3	2	1	0
DIRQ1	DIRQ0	CIRQ1	CIRQ0	BIRQ1	BIRQ0	AIRQ1	AIRQ0

DIRQ1 When this bit is set, the 8255 in Group 3 will generate an interrupt on INTRB if INTEN in BADR + 15 hex is also set.

DIRQ0 When this bit is set, the 8255 in Group 3 will generate an interrupt on INTRA if INTEN in BADR + 15 hex is also set.

CIRQ1 When this bit is set, the 8255 in Group 2 will generate an interrupt on INTRB if INTEN in BADR + 15 hex is also set.

CIRQ0 When this bit is set, the 8255 in Group 2 will generate an interrupt on INTRA if INTEN in BADR + 15 hex is also set.

BIRQ1 When this bit is set, the 8255 in Group 1 will generate an interrupt on INTRB if INTEN in BADR + 15 hex is also set.

BIRQ0 When this bit is set, the 8255 in Group 1 will generate an interrupt on INTRA if INTEN in BADR + 15 hex is also set.

AIRQ1 When this bit is set, the 8255 in Group 0 will generate an interrupt on INTRB if INTEN in BADR + 15 hex is also set.

AIRQ0 When this bit is set, the 8255 in Group 0 will generate an interrupt on INTRA if INTEN in BADR + 15 hex is also set.

Interrupt Control 2

BADR3 + 15 hex

Read/Write

7	6	5	4	3	2	1	0
X	X	X	X	X	INTEN	CTRIR	CTR1

INTEN Enables or disables interrupt generation from the 82C55 chips.

1 = enabled

0 = disabled

CTRIR Enables or disables the counters as an interrupt source.

1 = counters may generate interrupts.

0 = counters cannot generate interrupts.

CTR1 Controls whether counter 2 is the interrupt source, or counter 1 is the interrupt source.

When CTR1 = 1, the interrupt source is counter 2 and counter 1 acts as a prescaler for counter 2.

When CTR1 = 0, the interrupt source is counter 1. (Counter 3 is not used.)

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