PCN

Due to obsolescence, the Realtek RTL8211E Ethernet PHY is being replaced by the Realtek RTL8211F on several Digilent products starting the PCA revisions listed in the table below.

The RTL8211F is not functionally equivalent to the RTL8211E and might require changes to customer applications (embedded software) depending on the board support package in use (OS, drivers and libraries).

A non-exhaustive list of the changes in RTL8211F vs. RTL8211E:

- PHYSR1 (PHY Specific Status Register 1) at Page 0xA43, Address 0x1A vs. PHYSR at Address 0x11. Register field layout also differs. Affected functionality includes auto-negotiated speed, duplex and link detection.
- INSR (Interrupt Status Register) at Page 0xA43, Address 0x1D vs. INSR at Address 0x13. Register field layout also differs. Affected functionality is interrupt detection.
- INER (Interrupt Enable Register) power-on defaults to only the PHY Register Accessible Interrupt being enabled vs. all interrupt sources enabled. Interrupt sources must now be explicitly enabled, if required.
- Power-on sequencing requirements changed. The RTL8211F now regulates its own core voltage, as its internal regulator cannot be turned off. The 1.8V I/O voltage sequencing requirements forced all I/O circuitry in bank 501 (Ethernet, USB, UART, SD) to be separated from the main 1.8V board supply by a load switch. This I/O supply is now the last in the sequence to power-on. The board power-on reset circuitry required to be changed as well. Power-on now takes more time.
- Power-on core logic ready time 100 ms vs. 20 ms. The RTL8211F reserves a 100 ms window after power-on that is not being used for now. The only register access allowed in this window is Page 0xa46, Reg. 20, bit[1]=1 (PHY Special Config Done), to skip this window and enter normal operating state. Otherwise, the PHY will do it automatically when the wait period ends. Entering normal operating state is signaled by the ETH_INT_B interrupt. This behavior affects only very short boot time applications, which have been explicitly optimized for this purpose. Such applications must make sure they monitor the PHY interrupt and do not access any registers other than the one stated above before the Special Config Done even arrives.
  The typical boot time of a small non-optimized stand-alone application from the QSPI flash is 86 ms from the de-assertion the PS_POR_B signal. The PS_POR_B delay was increased and the PHY is now taken out of reset ahead of the Zynq. Therefore, without specific boot time optimizations, the RTL8211F is guaranteed to be ready by the time the software needs it.
- Three PHY status LEDs vs. two. The Link and Activity LEDs have been replaced by one LED for each link speed that integrate link and activity. These are now labeled “10”, “100”, and “1G”.

Embedded software work-arounds depending on the board support package:

- Stand-alone environments are expected to be using Xilinx’s lwip library with built-in PHY support for the RTL8211E. This will need to be replaced by a modified library that adds support for the RTL8211F. The patched library is published on Digilent’s Github page: https://github.com/Digilent/embeddedsw/tree/realtek-21.1. It is expected to be upstreamed to Xilinx in a future Vitis version.

If the ETH_INT_B interrupt is used in the application, the necessary interrupt sources must now be enabled explicitly.
If the application optimizes boot time, the PHY needs to be initialized by writing Page 0xa46, Reg. 20, bit[1]=1 (PHY Special Config Done).

- U-boot and Linux kernel built using Petalinux 2016.1 or later support RTL8211F with no changes necessary.

Affected products:

Product Name	SKU	First PCA revision with RTL8211F
Zybo Z7-10	410-351-10	D.0
Zybo Z7-20	410-351-20	D.0
Arty Z7-10	410-346-10	D.0
Arty Z7-20	410-346-20	TBD
PYNQ-Z1	6003-410-017	F.0