Overcoming Sampling Rate Limitations

Using Digilent's Eclypse Z7

Introduction

In applications ranging from radar to radio, band-limited analog signals are often digitized at relatively high sampling rates. The downstream implications of these high sampling rates impose limitations on system design that negatively impact cost, energy efficiency, and overall simplicity. Fortunately, a variety of digital signal processing techniques and hardware building blocks have been developed to overcome these limitations, allowing designers to prototype and design highly performant products quickly.

Multi-Rate Digital Signal Processing

Generally speaking, most analog signals of interest are bandlimited. This implies that the information contained within these signals has a finite span of frequency content that can be shifted up and down the frequency spectrum. Traditional AM/FM radio broadcasting is an excellent example, where a high-frequency carrier is modulated with bandlimited audio information. Mixers and filters can be deployed to shift the center frequency of the signal effectively to recover the baseband signal from the modulated carrier. The following figure depicts the classic super-heterodyne technique using a mixer and an intermediate frequency (IF) local oscillator to shift the signal of interest (S1) down to a lower center frequency.

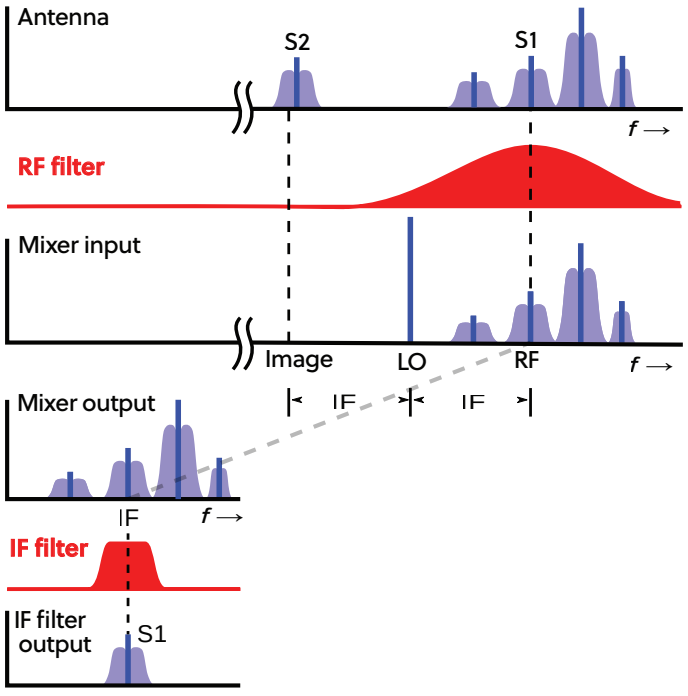

Figure 1: Traditional Superheterodyne Receiver (Wikipedia)

Performing this type of frequency shifting in multiple stages can effectively shift the signal of interest to the baseband for information recovery. For decades, this has been the primary strategy used in the vast majority of radio frequency transmitters and receivers. More recently, with advancements in high-speed integrated circuits, direct sampling has taken center stage as the preferred alternative. In the direct sampling scheme, the signal of interest (S1) can be sampled wherever it may lie in the frequency spectrum. The only requirement is that the sampling circuits adhere to Nyquist limits and that the input spectrum is bandlimited or filtered to prevent aliasing. Once the target signal has been digitized, all of the remaining frequency shifts and demodulation can be performed digitally, which is the basis for software-defined radio (SDR) or, more generally, digital down-conversion.

Digital Down-Converter System

While it is theoretically possible to just process the sampled signal directly, this would be highly inefficient and difficult to achieve in practice. Instead, the sampled signal can be down-converted to a lower sampling rate without any information loss to alleviate the requirements of processing power and high-speed PCB design. Down-conversion in the digital domain adheres to all the same rules as in the analog domain. As shown in the figure below, the digital equivalent of mixing can be performed by taking the high-speed sampled signal and multiplying it by a digital sine or cosine waveform. The resulting signal and image can then be digitally filtered and the sampling rate decimated to create a digital version of the frequency shifted input.

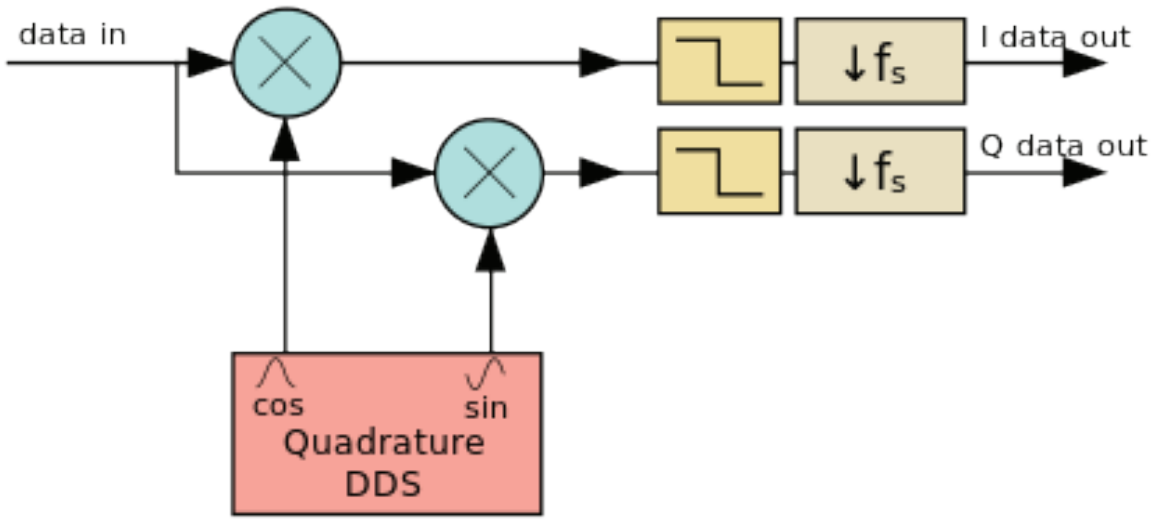

Figure 2: Digital Down-Convertor Block Diagram

Down-converting in the digital domain is much simpler and more flexible than mixing and filtering in the analog domain. It does, however, require some highly specialized hardware to bridge the analog and digital boundary.

As previously mentioned, directly sampling a high-speed signal requires oversampling by at least the Nyquist rate and, more practically, somewhere around 5-10 times the Nyquist rate. For example, an AM radio station centered at 930kHz would require direct sampling at around 4-9 MSPS. As the center frequency increases, the requirements on the analog-to-digital converter (ADC) become more and more difficult. Modern ADCs are now capable of multi-gigasample per second data rates at 12 to 14 bits of resolution, enabling direct to digital sampling of a wide variety of radio, radar, and oscilloscope applications.

Once the signal of interest is sampled, a massive quantity of high-speed digital data must then be accounted for. This process requires high-speed differential signaling on parallel lines and careful timing with an FPGA to accurately receive, buffer, and process the data. The top-level block diagram of such a system is shown in the figure below.

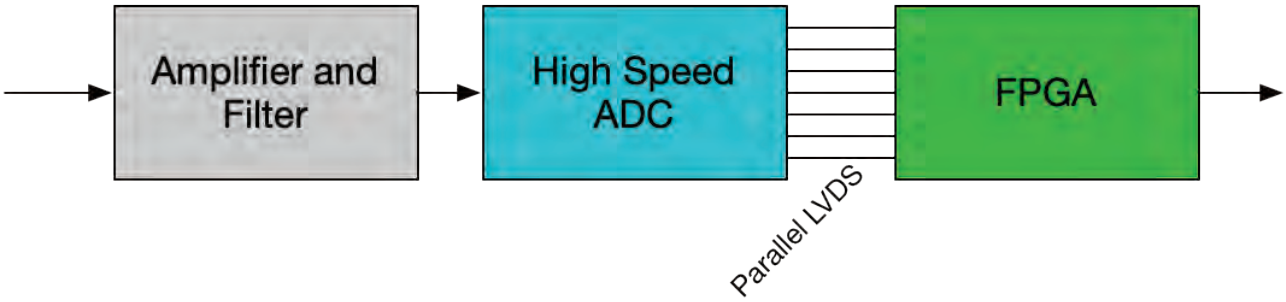

Figure 3: Direct Digital Sampling Front End

The Digilent Eclypse Z7

When it comes to designing and prototyping a directly sampled signal processing system, the upfront requirements for sampling rate and FPGA capability may be difficult to determine. Often, the best course of action is to begin with an over-engineered off-the-shelf solution to refine the top-level system specifications. The Digilent Eclypse Z7 is just such a platform, as shown in the figure below.

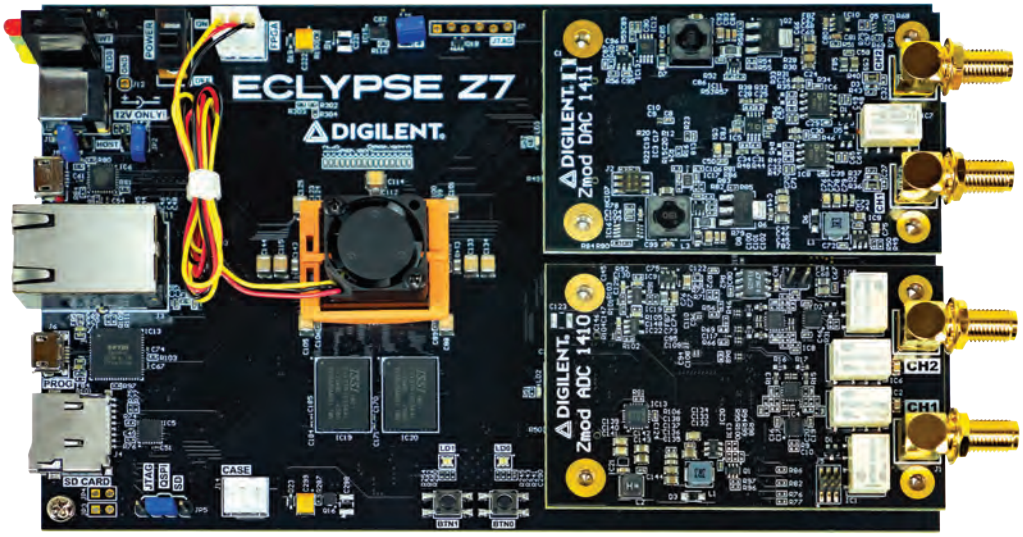

Figure 4: Digilent "Eclypse Z7" Main Board

At the heart of the Z7 is the Zynq-7000 APSoC, offering a 667 MHz dual-core Cortex-A9 processor and programmable logic equivalent to Artix-7 FPGA. This powerhouse combination is supported by a wide variety of peripherals, including a DRAM controller, a Flash controller, and various standard serial transceivers, to name a few. Most importantly, the programmable logic portion of the chip includes interfaces for high-speed data transfer. Of particular interest are the two SYZYGY ports, each containing eight differential I/Os for communicating with high-speed ADCs and DACs. The top-level block diagram is shown in the figure below.

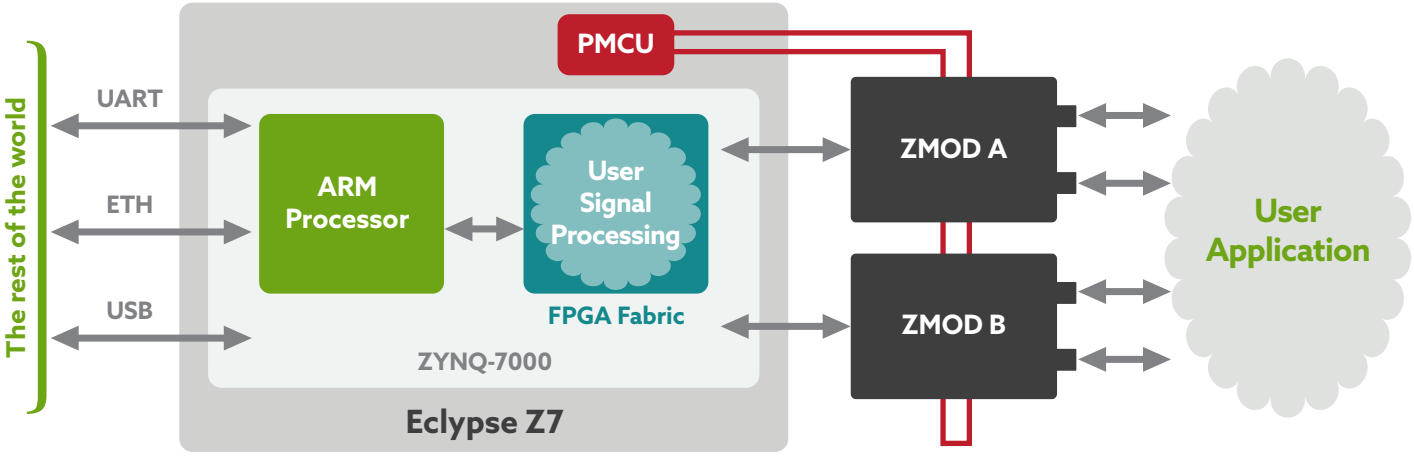

Figure 5: Zynq-7000 APSoC block diagram

The Eclypse Z7 also provides the supporting circuitry needed, such as power, programming interfaces, and connectivity options, to ensure that designers can bring any prototype to life as quickly as possible. The flexibility and processing power of such a development system enables the designer to focus only on the core requirements of their signal acquisition system without introducing hardware constraints that might otherwise consume too much focus.

Example Signal Acquisition System

Two additional off-the-shelf modules will be leveraged to demonstrate how the Eclypse Z7 can be used to build a digital down-conversion prototype quickly. The first is the Zmod Scope ADC, shown in the figure below.

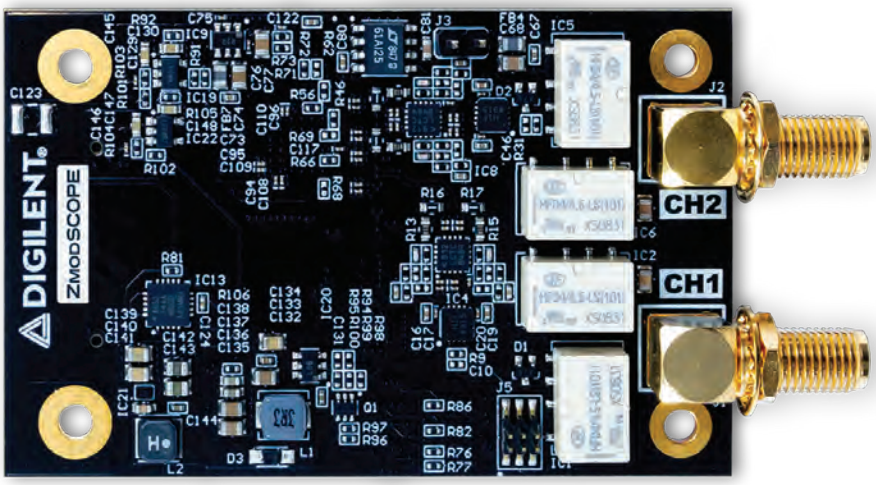

Figure 6: Digilent "ZmodScope" Analog To Digital Converter

The Zmod Scope uses a dual channel, high speed, low power, 14-bit, 105MS/s ADC, and connects readily to the Z7 using one of the SYZYGY ports. Such an ADC provides the dynamic range and sampling speed to prototype a wide variety of signal acquisition concepts.

The second module used is the Zmod AWG, a 14-bit arbitrary waveform generator also connected to one of the Z7 SYZYGY ports. Though not technically required for digital down-conversion, this AWG is quite useful for getting data back out from the Z7 for analysis in the analog domain. A basic acquisition system is shown in the figure below, where a network analyzer is used to create a signal for acquisition and also analyze the output from the AWG to gain insight into frequency content and phase delay.

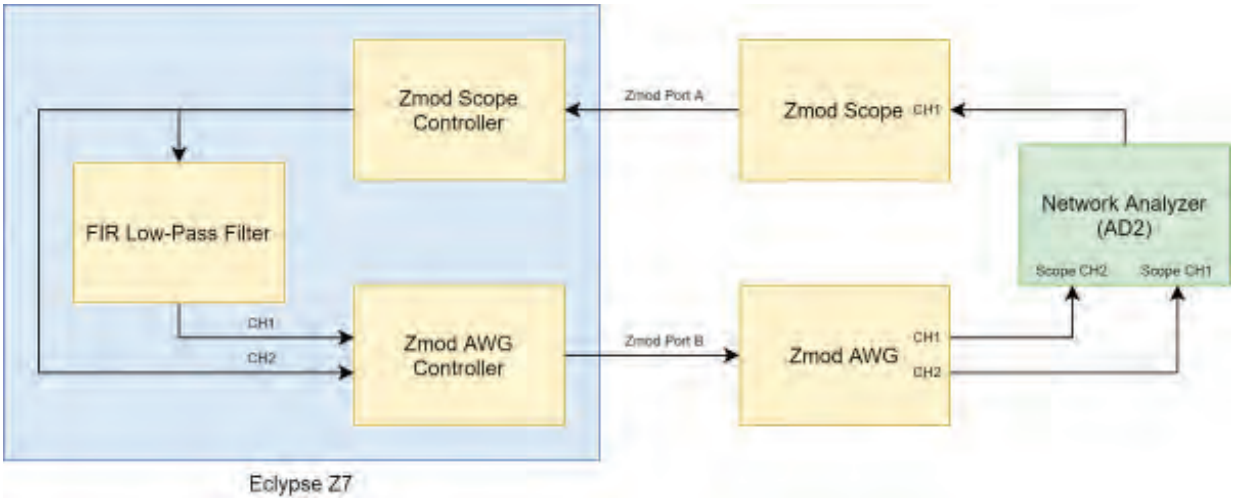

Figure 7: Signal Acquisition System

This entire acquisition system can be implemented using three simple IP blocks that reside solely in the programmable logic portion of the Zynq-7000: a Zmod scope controller, a digital FIR filter, and a Zmod AWG controller. To extend this example for performing full digital down conversion, one would only need to add multiplication, low-pass filter, and decimation blocks and then route the resulting data into the processor for application use.

The Digilent Eclypse Z7

Digital down-conversion is a mainstay for modern signal acquisition systems focused on simplicity and performance. This technique effectively walls off the high-speed sampling requirements using an ADC and FPGA to alleviate the constraints placed upon the rest of the processing system. Unfortunately, prototyping and specifying such a design can be quite arduous owing to the number of variables and complexity of the associated hardware. A highly performant development platform, like Digilent's Eclypse Z7, can pave the way for a speedy and painless design process, yielding a final system design optimized for sampling and processing requirements. To learn more, visit the Z7 product page.

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